

PAGE	CONTENTS
1	INDEX
2	BLOCK DIAGRAM
3	POWER DELIVERY
4	RESERVED FOR CK505 CLOCK GEN
5	CPU PCIEX16/DMI/FDI
6	CPU DDR CHANNEL A
7	CPU DDR CHANNEL B
8	CPU MISC
9	CPU POWER & GND
10	DDR3 DIMMA1/A2
11	DDR3 DIMMB1/B2
12	PCH PCI
13	PCH DMI/PCIE/USB
14	PCH CLINK/SATA/CPU HOST
15	PCH LPC/HDA/SPI/MISC
16	PCH NVRAM & FDILINK
17	PCH VGA/DISPLAY PORT
18	PCH CLOCK BUFFER
19	PCH POWER
20	PCH GND
21	SPI ROM/BAT
22	PCIEX16 SLOT
23	PCIEX4/X1 SLOT
24	RESERVED FOR PCI BRIDGE
25	RESERVED FOR PCI SLOT
26	VGA/DVI CONNECTOR
27	HDMI PORT
28	RESERVED FOR 1394
29	AUDIO CODEC ALC662
30	AUDIO CONNECTOR
31	LAN RTL8111E/8105E
32	SUPERIO ITE8728
33	SUPERIO PS2/COM/PRINTER
34	SUPERIO FAN CONTROL
35	USB2.0 PORT
36	24PIN POWER CONN&FP
37	RESUME RESET LOGIC
38	ACPI POWER CONTROL
39	LINEAR POWER
40	MEMORY DC-DC Conver
41	VTT DC-DC Conver
42	VCORE VREG1
43	VCORE VREG2
44	OVER VOLTAGE
45	RESERVED FOR AMT POWER
46	USB3.0 PORT
47	BOM

IH77A-MHS H77MH REV 6.0

CPU:

Intel Sandy/Ivy Bridge processors in LGA1155 Package 95W

System Chipset:

Panther Point H77

Main Memory:

Dual Channel/DDR-III*4(Max 32GB) 1066/1333

DDR3-1333 /1066 /800

Onboard Device:

Super I/O:IT8728

LAN:Realtek 8111EL

HD Codec:ALC662 3 jacks

Power solution:

CPU Voltage Regulators:3phase by ISL6363

AXG voltage Regulators:1phase by ISL6363

VTT voltage Regulators:1Phase by FP6326

DDR voltage Regulators:1Phase by FP6326

Expansion Slots:

PCI EXPRESS 16X SLOT*1

PCI EXPRESS 4X SLOT*1

PCI EXPRESS 1X SLOT*2

REAR I/O:

PS/2 +2 layer USB2.0 Port

HDMI Port

DVI Port

VGA Port

2 layer USB3.0 + Gb RJ-45 Ports

Audio Jackets

Front I/O:

SATA2 * 4

SATA3 * 2

USB2.0 Header * 2

USB3.0 Header * 1

CPU /System1

CIR Header


Front Audio Header

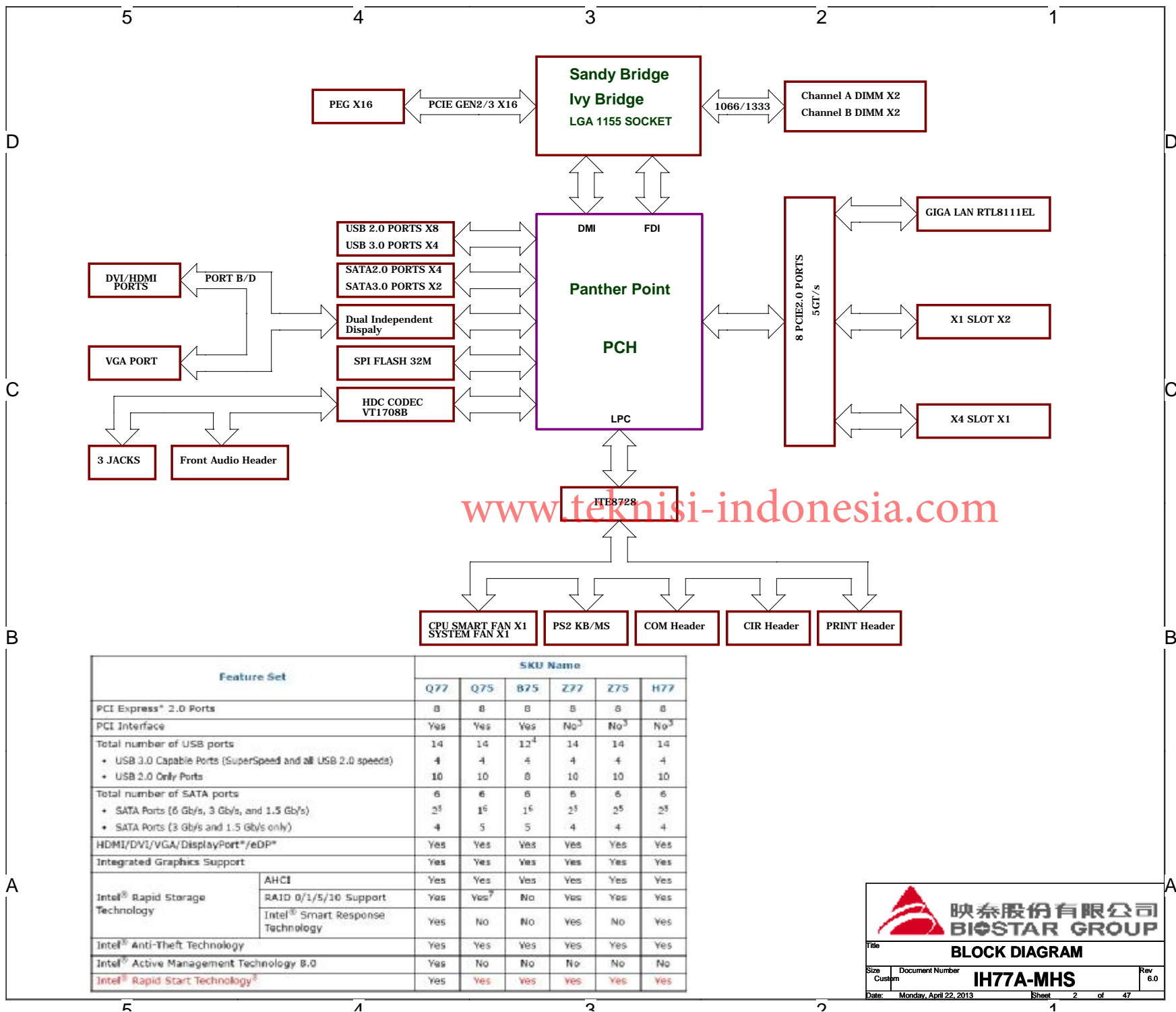
I/O Panel:

47-RIOBRACKET-95A


HW Engineer		Date	
HW Leader1		Date	
HW Leader2		Date	

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Title INDEX			
Size Custom	Document Number IH77A-MHS		Rev 6.0
Date: Monday, April 22, 2013	Sheet 1	of 47	



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Title CHANGE LIST		
Size B	Document Number IH77A-MHS	Rev 6.0
Date: Monday, April 22, 2013		
Sheet 3 of 47		

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Title RESERVED		
Size B	Document Number IH77A-MHS	Rev 6.0
Date: Monday, April 22, 2013 Sheet 4 of 47		

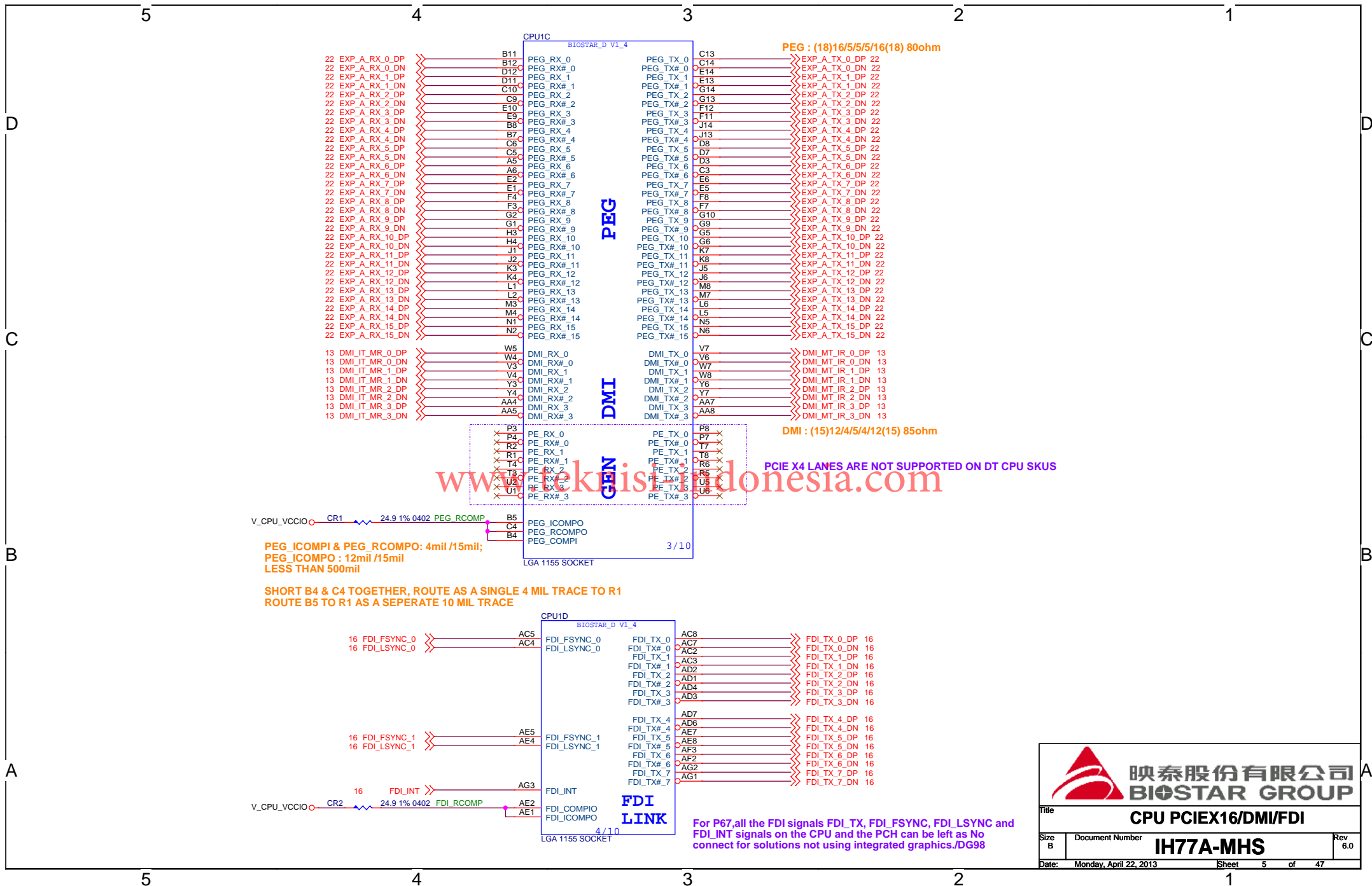
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DQ REMAPPING IMPLEMENTED
TO IMPROVE BREAKOUT AND
MINIMIZE CH-2-CH COUPLING

DQ REMAPPING IMPLEMENTED
TO IMPROVE BREAKOUT AND
MINIMIZE CH-2-CH COUPLING

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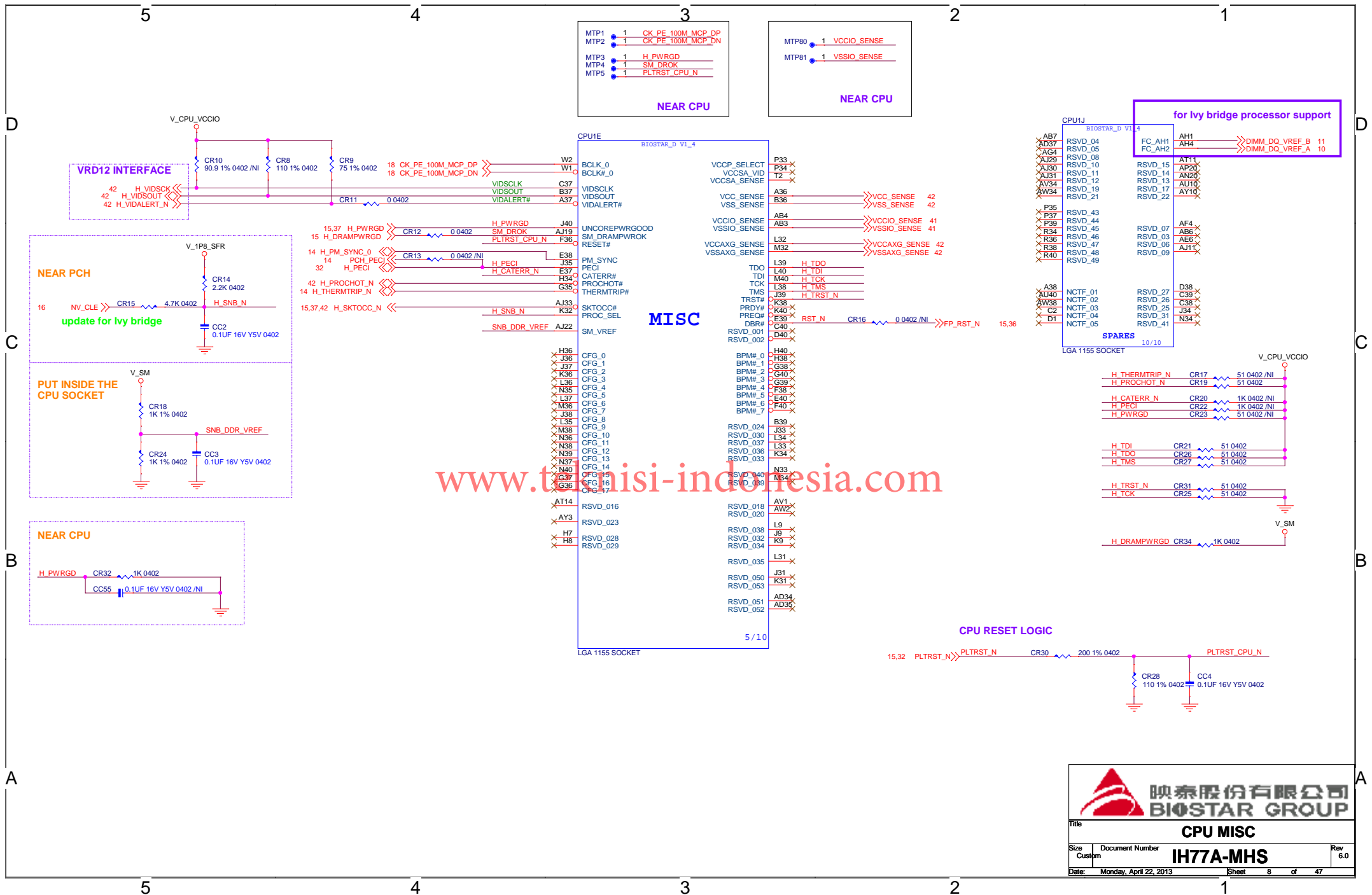
11 M_DQS_B_DP0<<< AH7 SB_DQS_0
11 M_DQS_B_DP1<<< AM8 SB_DQS_1
11 M_DQS_B_DP2<<< AR8 SB_DQS_2
11 M_DQS_B_DP3<<< AN13 SB_DQS_3
11 M_DQS_B_DP4<<< AN29 SB_DQS_4
11 M_DQS_B_DP5<<< AP33 SB_DQS_5
11 M_DQS_B_DP6<<< AL33 SB_DQS_6
11 M_DQS_B_DP7<<< AG35 SB_DQS_7

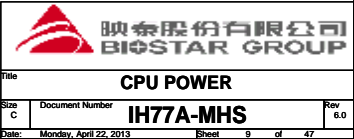
11 M_DQS_B_DN0<<< AH6 SB_DQS#_0
11 M_DQS_B_DN1<<< AL8 SB_DQS#_1
11 M_DQS_B_DN2<<< AP8 SB_DQS#_2
11 M_DQS_B_DN3<<< AN12 SB_DQS#_3
11 M_DQS_B_DN4<<< AN28 SB_DQS#_4
11 M_DQS_B_DN5<<< AR33 SB_DQS#_5
11 M_DQS_B_DN6<<< AM33 SB_DQS#_6
11 M_DQS_B_DN7<<< AG34 SB_DQS#_7

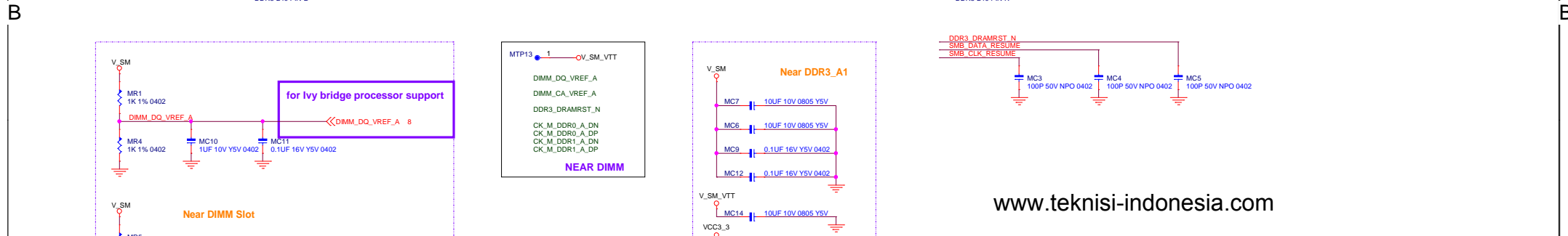
CPU1B
BIOSTAR_D_V1_4
SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14
SB_MA_15
SA_CK(2)
SA_CK(1)
SA_ODT(2)
SB_BS_0
SB_BS_1
SB_BS_2
SB_CS#_0
SB_CS#_1
SB_CS#_2
SB_CS#_3
SB_CKE_0
SB_CKE_1
SB_CKE_2
SB_CKE_3
SB_ODT_0
SB_ODT_1
SB_ODT_2
SB_ODT_3
SB_CK#_0
SB_CK#_1
SB_CK#_2
SB_CK#_3
SB_DQS_8
SB_DQS#_8
SB_ECC_CB_0
SB_ECC_CB_1
SB_ECC_CB_2
SB_ECC_CB_3
SB_ECC_CB_4
SB_ECC_CB_5
SB_ECC_CB_6
SB_ECC_CB_7
LGA 1155 SOCKET

DDR_1
2 / 10

M_MAA_B[0..15] 11
AK24 M_MAA_B0
AM20 M_MAA_B1
AM19 M_MAA_B2
AK18 M_MAA_B3
AP19 M_MAA_B4
AP18 M_MAA_B5
AM18 M_MAA_B6
AL18 M_MAA_B7
AN18 M_MAA_B8
AY17 M_MAA_B9
AN23 M_MAA_B10
AU17 M_MAA_B11
AT18 M_MAA_B12
AR26 M_MAA_B13
AY16 M_MAA_B14
AV16 M_MAA_B15
AR25 M_WE_B_N 11
AK25 M_CAS_B_N 11
AP24 M_RAS_B_N 11
AP23 M_SBS_B0 11
AM24 M_SBS_B1 11
AW17 M_SBS_B2 11
AN25 M_SCS_B_N0 11
AN26 M_SCS_B_N1 11
AL25 M_SCS_B_N2 11
AT26 M_SCS_B_N3 11
AU16 M_SCKE_B0 11
AY15 M_SCKE_B1 11
AW15 M_SCKE_B2 11
AV15 M_SCKE_B3 11
AL26 M_ODT_B0 11
AP26 M_ODT_B1 11
AM26 M_ODT_B2 11
AK26 M_ODT_B3 11
AL21 CK_M_DDR0_B_DP 11
AL22 CK_M_DDR0_B_DN 11
AL20 CK_M_DDR1_B_DP 11
AK20 CK_M_DDR1_B_DN 11
AL23 CK_M_DDR2_B_DP 11
AM22 CK_M_DDR2_B_DN 11
AP21 CK_M_DDR3_B_DP 11
AN21 CK_M_DDR3_B_DN 11
AN16
AN15
AL16
AM16
AP16
AR16
AL15
AM15
AR15
AP15









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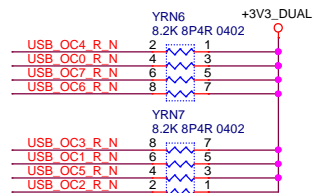
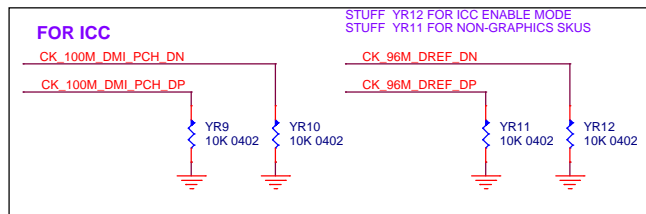
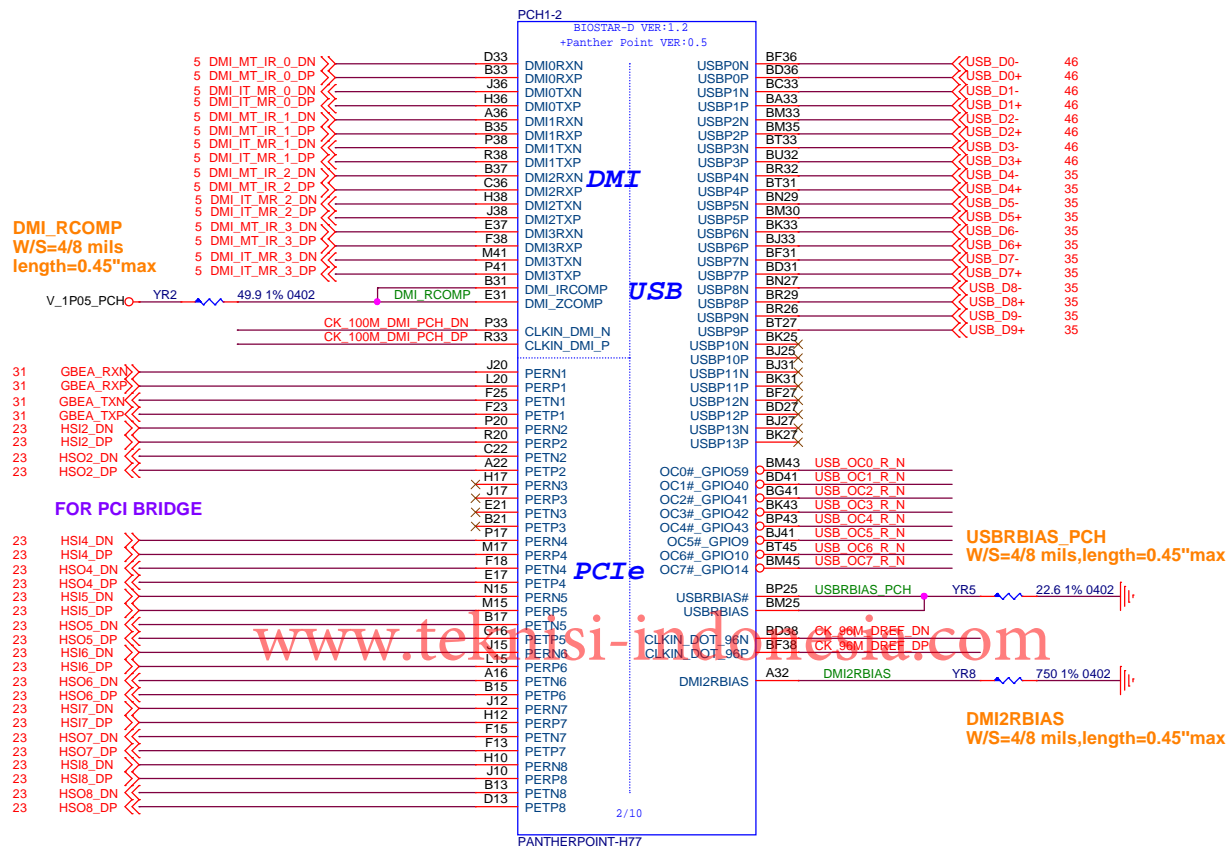
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映泰股份有限公司 BIOSTAR GROUP		
Title PCH DMI/PCIE/USB		
Size B	Document Number IH77A-MHS	Rev 6.0
Date Monday, April 22, 2013	Sheet 13 of 47	





PCH1-5

BIOSTAR-D VER:1.2
+Panther Point VER:0.5

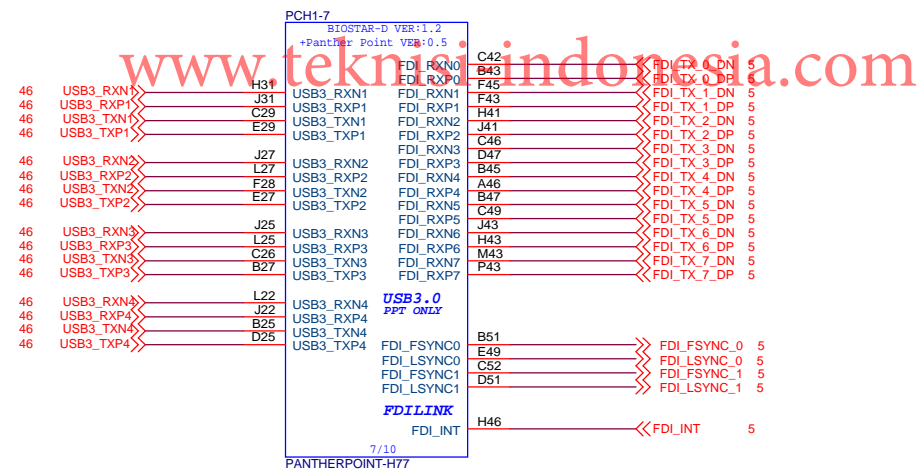
RSVD_29 RSVD_22 AB50
DF_TVS RSVD_21 Y50
RSVD_6 RSVD_14 AB49
RSVD_4 RSVD_13 AB48
RSVD_3 RSVD_12 U49
RSVD_2 RSVD_11 R44
RSVD_1 RSVD_10 U50
RSVD_9 U46
RSVD_8 U44
RSVD_7 H50
RSVD_20 K46
RSVD_19 J55
RSVD_18 F53
RSVD_17 H52
RSVD_16 E52
RSVD_15
RSVD_28 K50
RSVD_27 K49
RSVD_26 AB46
RSVD_25 G56
RSVD_24 Y44
RSVD_23 L53
RSVD_5 R50

NVRAM

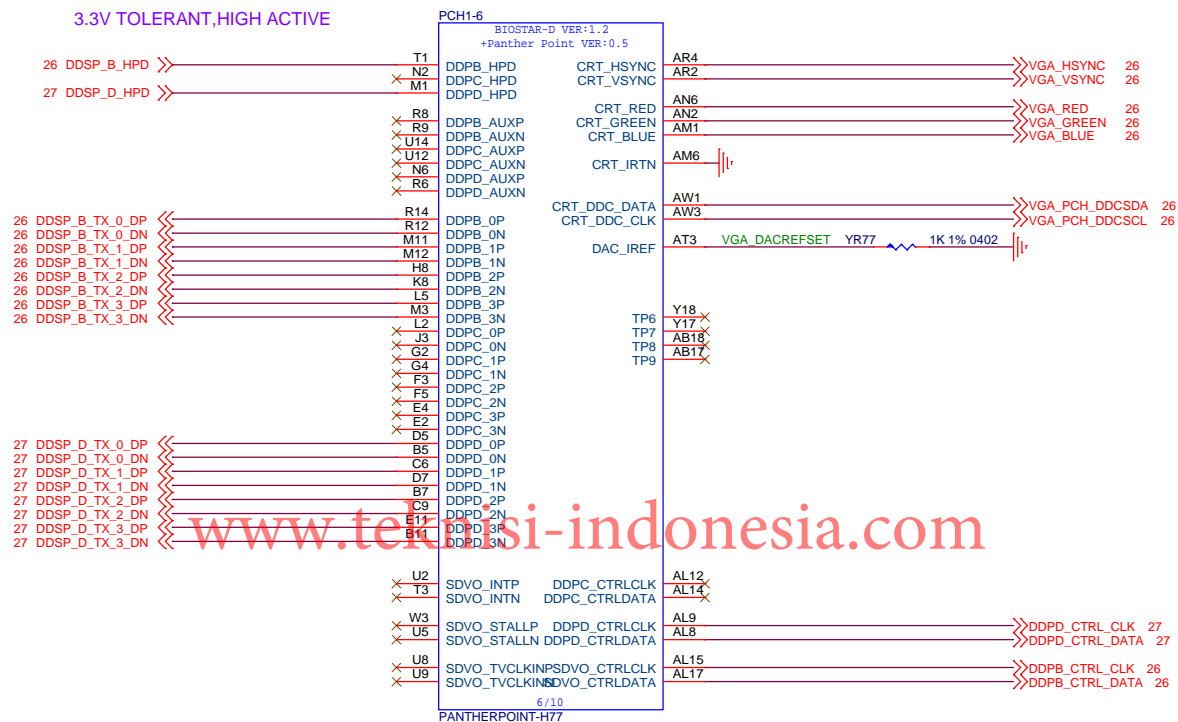
5/10

PANTHERPOINT-H77

NV_RCOMP YR74 33 0402 /NI



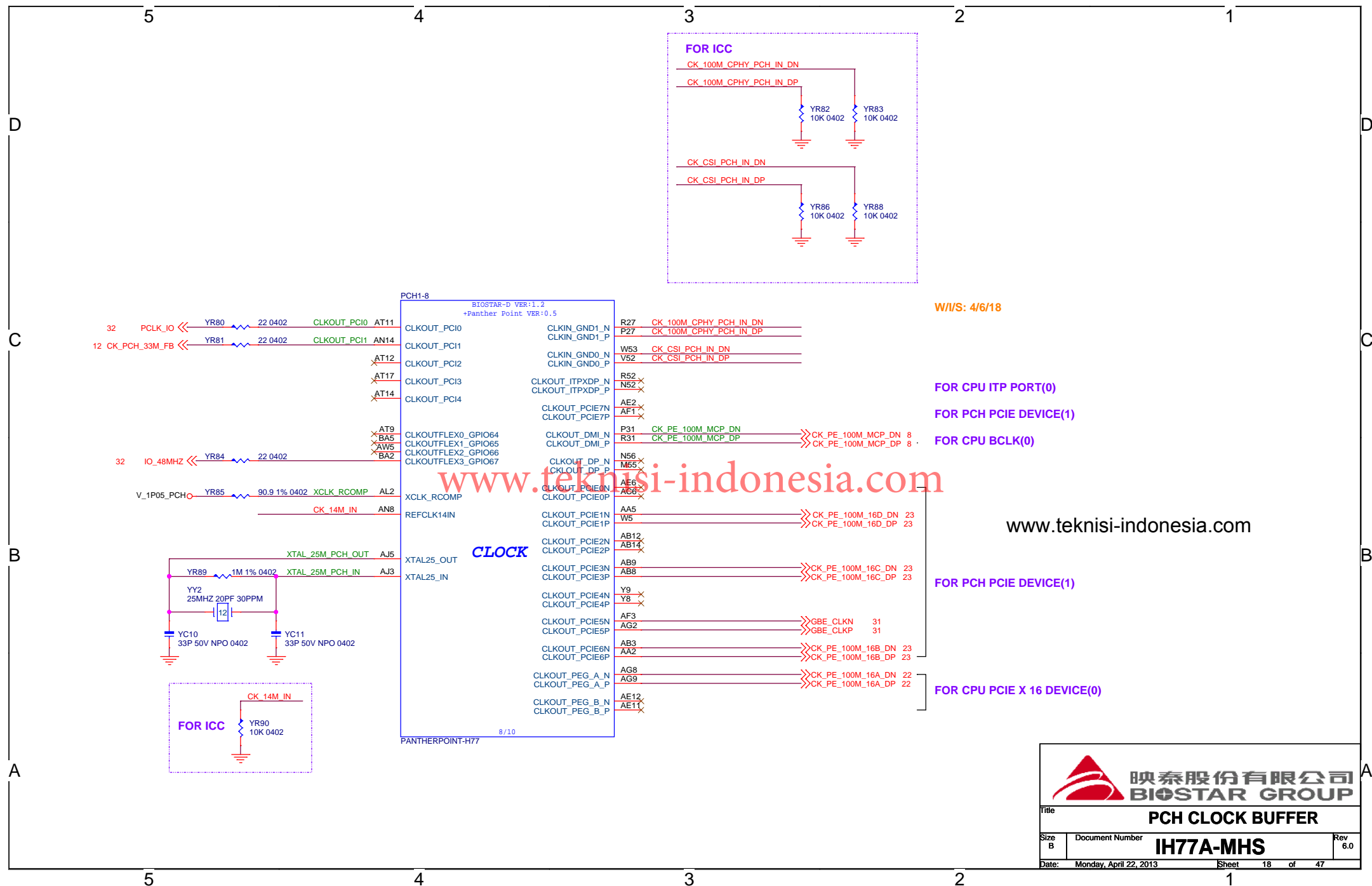
3.3V TOLERANT,HIGH ACTIVE

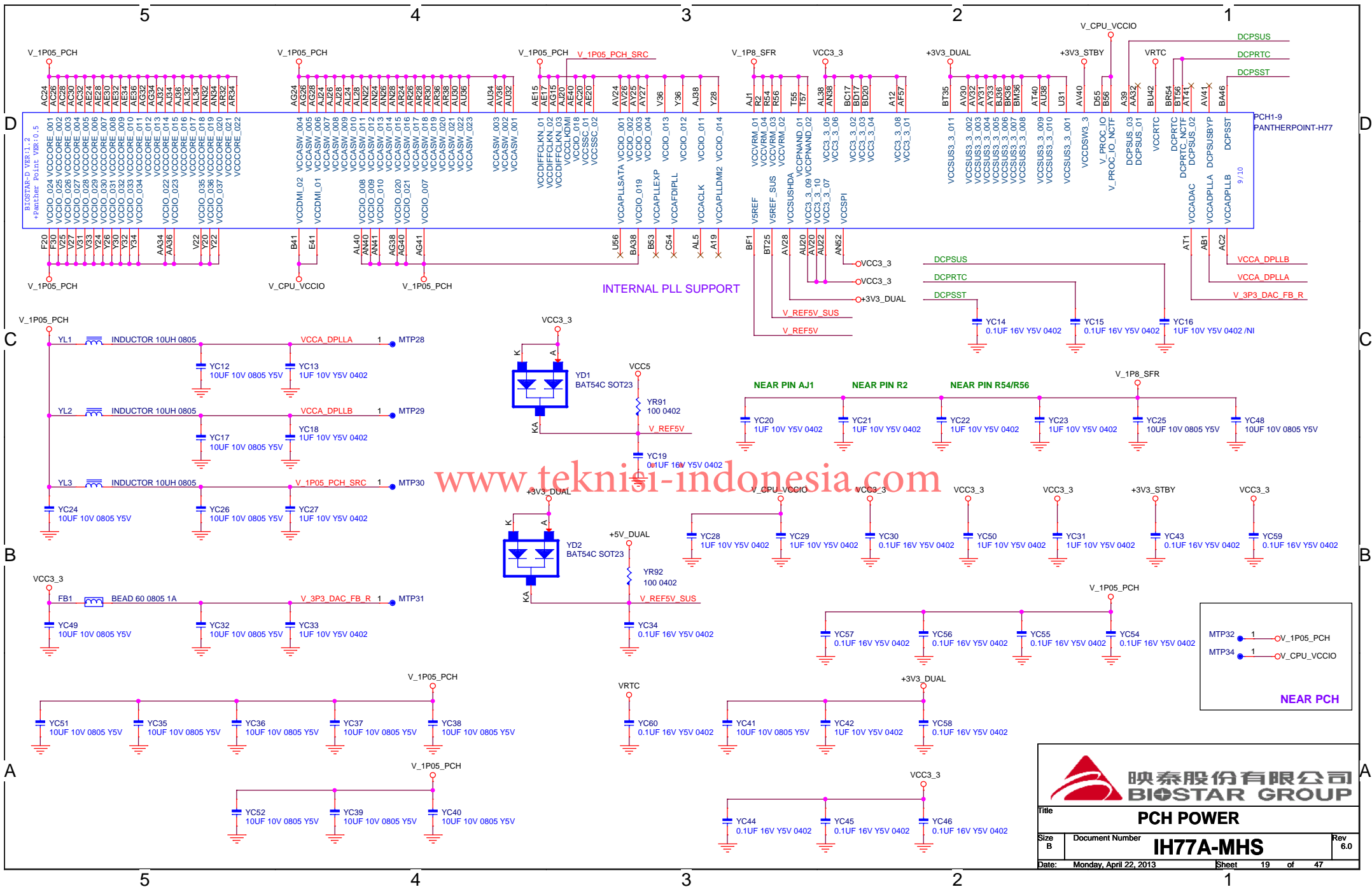


REMOVE LEVEL SHIFTER WHEN TRACE
LENGHT LESS THAN 9.25 INCHES

If DisplayPort interface is not implemented,
the Main Link, aux channel differential
signals and HPD signals can be left as No
Connects./DG108

		
映泰股份有限公司 BIOSTAR GROUP		
Title PCH VGA/DISPLAY PORT		
Size B	Document Number IH77A-MHS	Rev 6.0
Date: Monday, April 22, 2013	Sheet 17 of 47	





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Date:

Monday, April 22, 2013

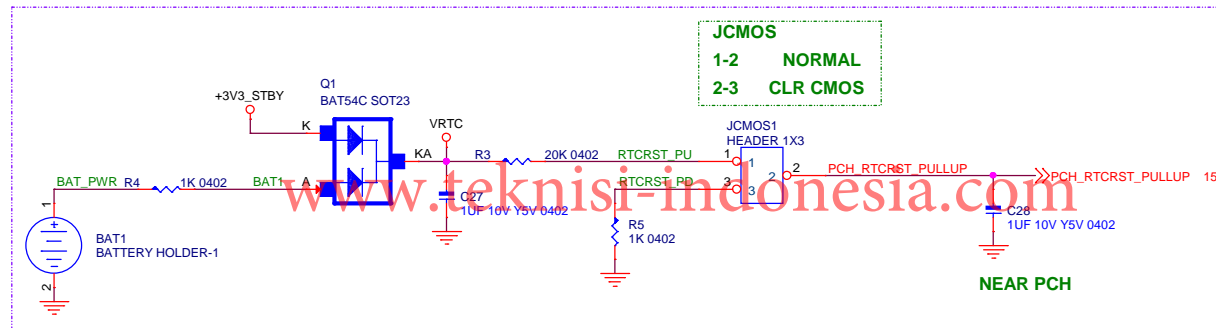
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20

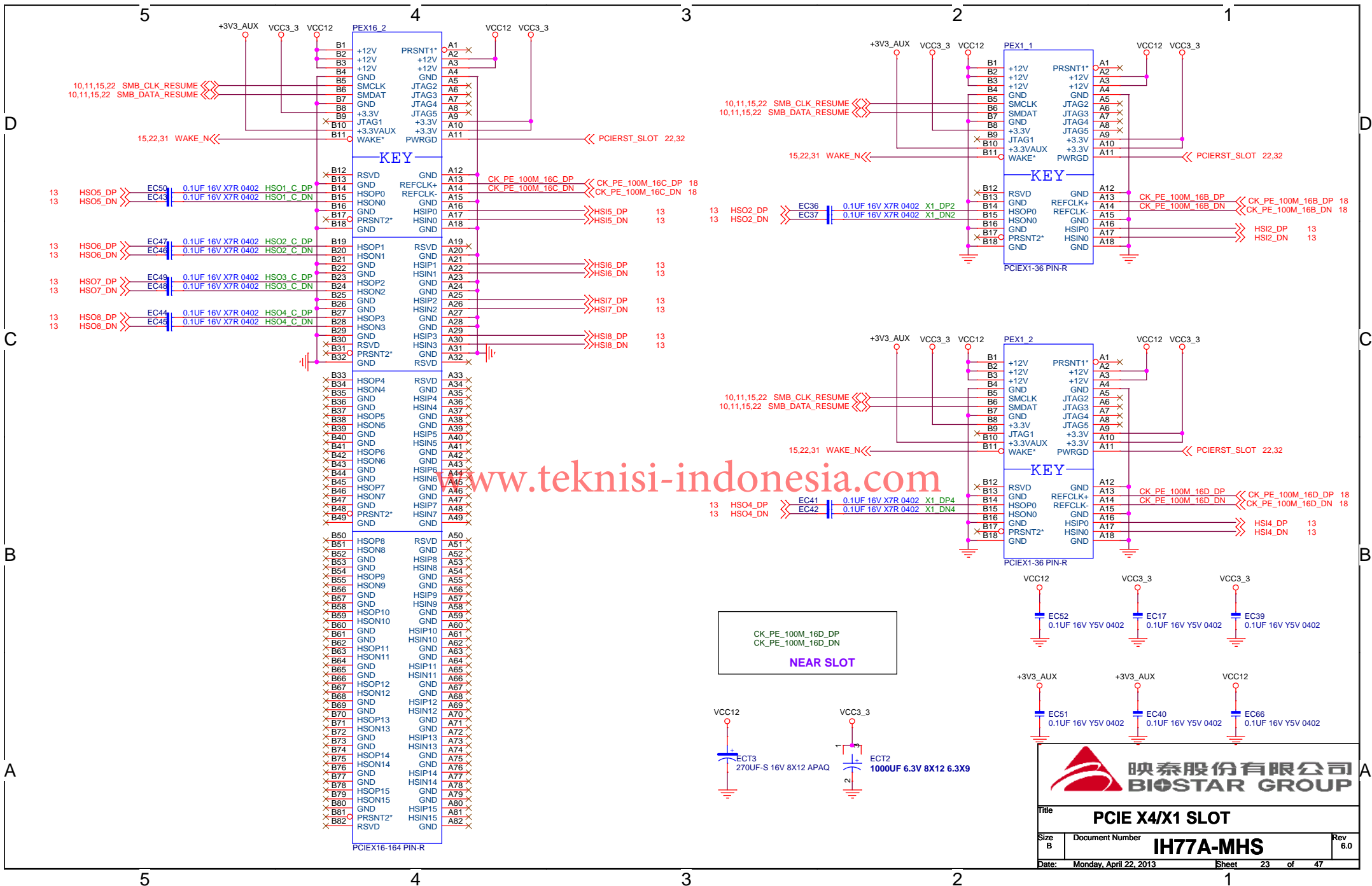
of

47

BC15	VSS_0126	426
BC20	VSS_0006	
BC21	VSS_0127	
BC23	VSS_0007	
BC26	VSS_0008	
BC27	VSS_0128	
BC28	VSS_0009	
BC29	VSS_0129	
BC30	VSS_0010	
BC31	VSS_0130	
BC32	VSS_0011	
BC33	VSS_0131	
BC34	VSS_0012	
BC35	VSS_0132	
BC36	VSS_0013	
BC37	VSS_0133	
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BC43	VSS_0136	
BC44	VSS_0017	
BC45	VSS_0137	
BC46	VSS_0018	
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BC49	VSS_0139	
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BC57	VSS_0143	
BC58	VSS_0024	
BC59	VSS_0144	
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BC63	VSS_0146	
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BC65	VSS_0147	
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BC85	VSS_0207	
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BC08	VSS_0099	
BC09	VSS_0219	
BC10	VSS_0100	
BC11	VSS_0220	
BC12	VSS_0101	
BC13	VSS_0221	
BC14	VSS_0102	
BC15	VSS_0222	
BC16	VSS_0103	
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BC33	VSS_0231	
BC34	VSS_0112	
BC35	VSS_0232	
BC36	VSS_0113	
BC37	VSS_0233	
BC38	VSS_0114	
BC39	VSS_0234	
BC40	VSS_0115	
BC41	VSS_0235	
BC42	VSS_0116	
BC43	VSS_0236	
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BC45	VSS_0237	
BC46	VSS_0118	
BC47	VSS_0238	
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BC49	VSS_0239	
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BC51	VSS_0240	
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BC76	VSS_0133	
BC77	VSS_0253	
BC78	VSS_0134	
BC79	VSS_0254	
BC80	VSS_0135	
BC81	VSS_0255	
BC82	VSS_0136	
BC83	VSS_0256	
BC84	VSS_0137	
BC85	VSS_0257	
BC86	VSS_0138	
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BC64	VSS_0177	
BC65	VSS_0297	
BC66	VSS_0178	
BC67	VSS_0298	
BC68	VSS_0179	
BC69	VSS_0299	
BC70	VSS_0180	
BC71	VSS_0300	
BC72	VSS_0181	
BC73	VSS_0301	
BC74	VSS_0182	
BC75	VSS_0302	
BC76	VSS_0183	
BC77	VSS_0303	
BC78	VSS_0184	
BC79	VSS_0304	
BC80	VSS_0185	
BC81	VSS_0305	
BC82	VSS_0186	
BC83	VSS_0306	
BC84	VSS_0187	
BC85	VSS_0307	
BC86	VSS_0188	
BC87	VSS_0308	
BC88	VSS_0189	
BC89	VSS_0309	
BC90	VSS_0190	
BC91	VSS_0310	
BC92	VSS_0191	
BC93	VSS_0311	
BC94	VSS_0192	
BC95	VSS_0312	
BC96	VSS_0193	
BC97	VSS_0313	
BC98	VSS_0194	
BC99	VSS_0314	
BC00	VSS_0315	
BC01	VSS_0316	
BC02	VSS_0317	
BC03	VSS_0318	
BC04	VSS_0319	
BC05	VSS_0320	
BC06	VSS_0321	
BC07	VSS_0322	
BC08	VSS_0323	
BC09	VSS_0324	
BC10	VSS_0325	
BC11	VSS_0326	
BC12	VSS_0327	
BC13	VSS_0328	
BC14	VSS_0329	
BC15	VSS_0330	
BC16	VSS_0331	
BC17	VSS_0332	
BC18	VSS_0333	
BC19	VSS_0334	
BC20	VSS_0335	
BC21	VSS_0336	
BC22	VSS_0337	
BC23	VSS_0338	
BC24	VSS_0339	
BC25	VSS_0340	
BC26	VSS_0341	
BC27	VSS_0342	
BC28	VSS_0343	
BC29	VSS_0344	
BC30	VSS_0345	
BC31	VSS_0346	
BC32	VSS_0347	
BC33	VSS_0348	
BC34	VSS_0349	
BC35	VSS_0350	
BC36	VSS_0351	
BC37	VSS_0352	
BC38	VSS_0353	
BC39	VSS_0354	
BC40	VSS_0355	
BC41	VSS_0356	
BC42	VSS_0357	
BC43	VSS_0358	
BC44	VSS_0359	
BC45	VSS_0360	
BC46	VSS_0361	
BC47	VSS_0362	
BC48	VSS_0363	
BC49	VSS_0364	
BC50	VSS_0365	
BC51	VSS_0366	
BC52	VSS_0367	
BC53	VSS_0368	
BC54	VSS_0369	



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SPI ROM/BAT				
Size	Document Number			Rev
B	IH77A-MHS			6.0
Date:	Monday, April 22, 2013		Sheet	21 of 47



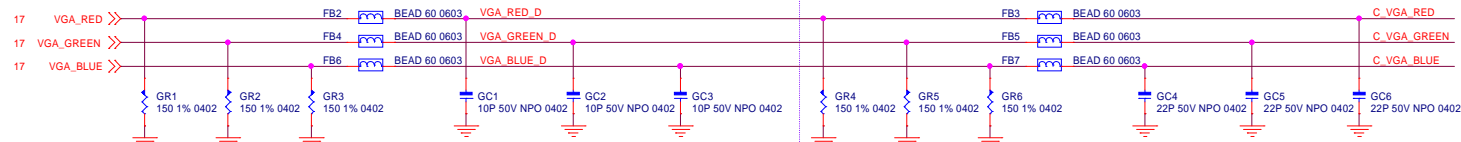
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Title		RESERVED FOR PCI BRIDGE	
Size B	Document Number IH77A-MHS		Rev 6.0
Date:	Monday, April 22, 2013		Sheet 24 of 47

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映泰股份有限公司 BIOSTAR GROUP		
Title RESERVED FOR PCI SLOT		
Size Custom	Document Number IH77A-MHS	Rev 6.0
Date: Monday, April 22, 2013	Sheet 25 of 47	

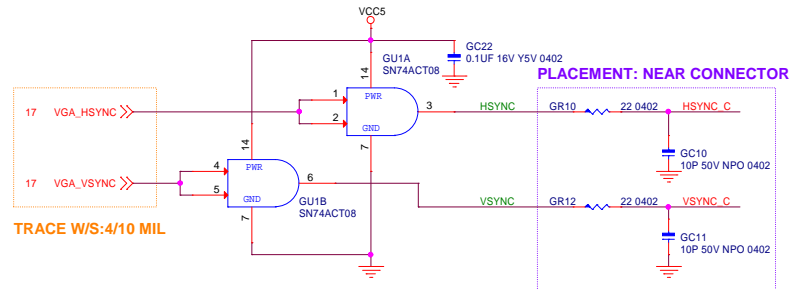


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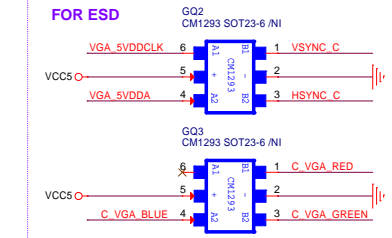
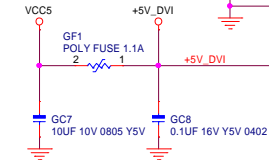
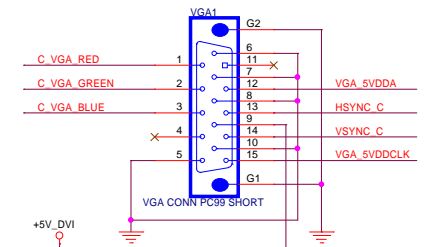
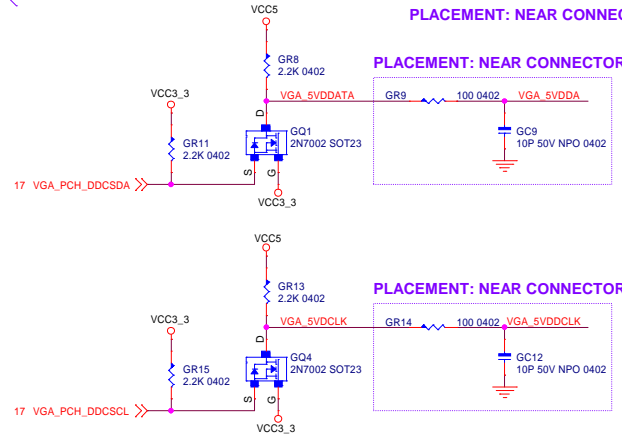
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TRACE W/S: 4/25 MIL (4/30 BETTER)

PLACEMENT: NEAR CONNECTOR

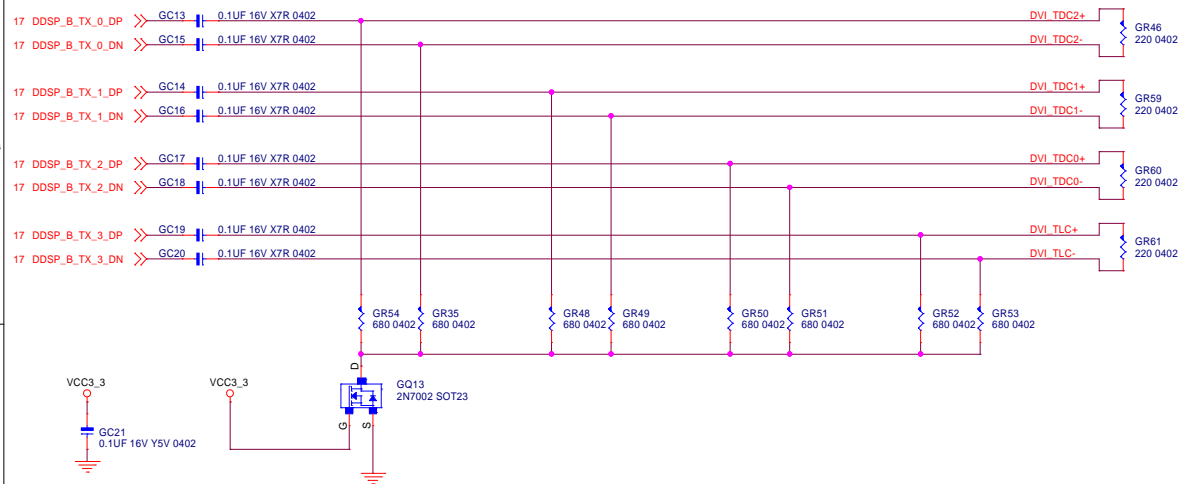


TRACE W/S: 4/10 MIL

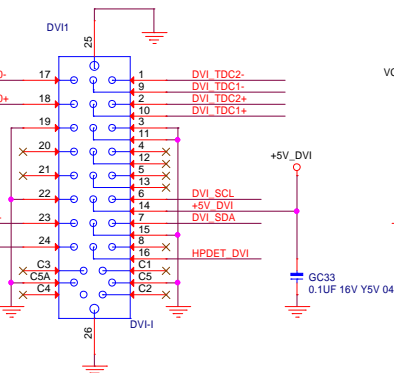


D_SUB

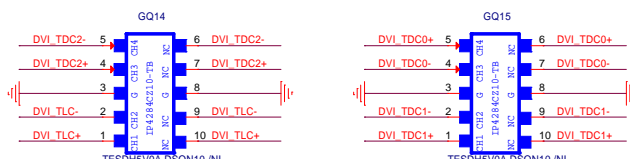
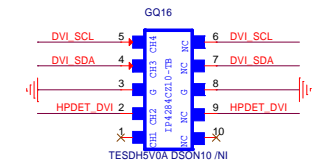
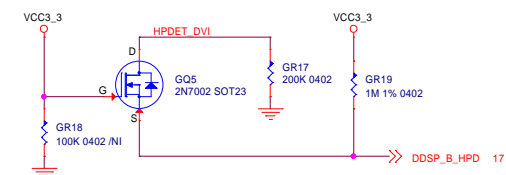
DVI



DVI CONNECTOR



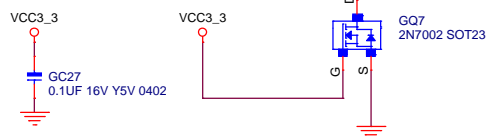
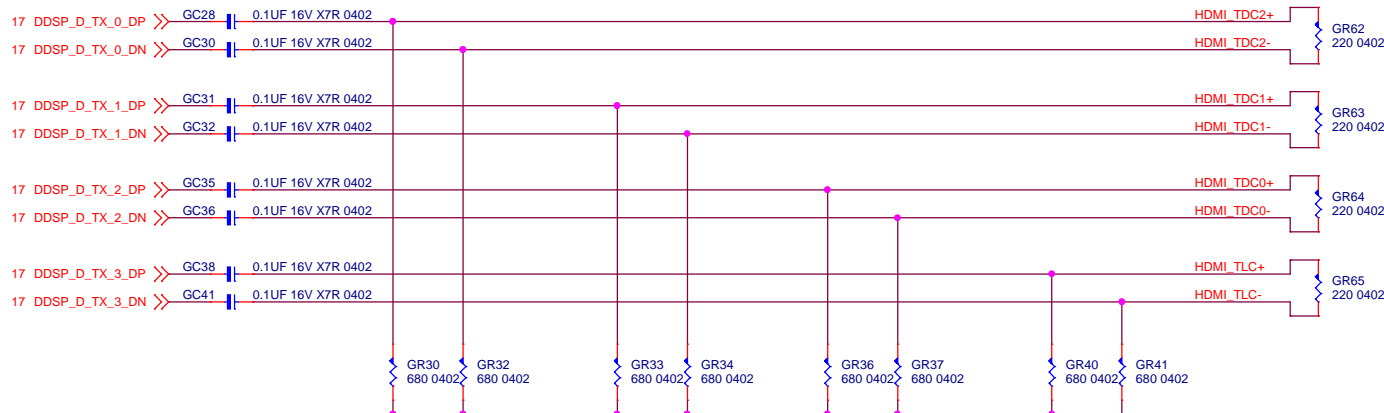
LEVEL SHIFTER HPD +5V SWITCH TO +3.3V



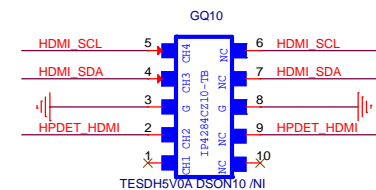
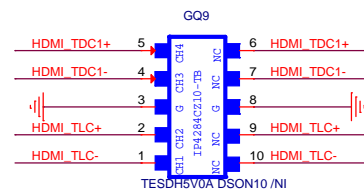
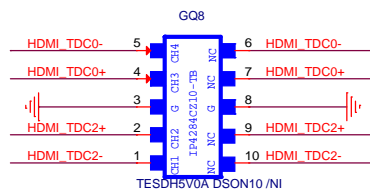
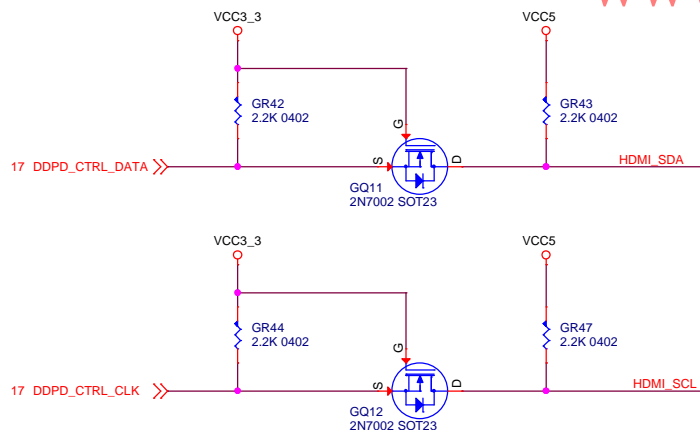
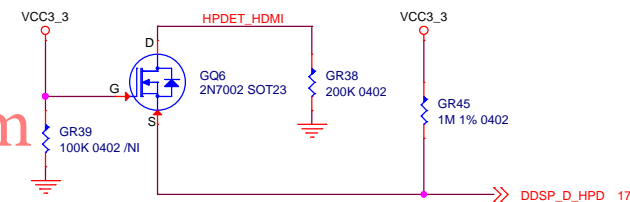
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BIOSAR GROUP

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Size	Document Number	IH77A-MHS	
Date:	Monday, April 22, 2013	Sheet	26 of 47

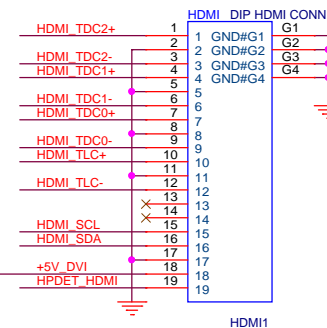
HDMI



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HDMI CONNECTOR



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BIOSTAR GROUP

Title: **HDMI**

Size B: **IH77A-MHS**

Document Number: **IH77A-MHS**


Date: Monday, April 22, 2013

Sheet: 27 of 47

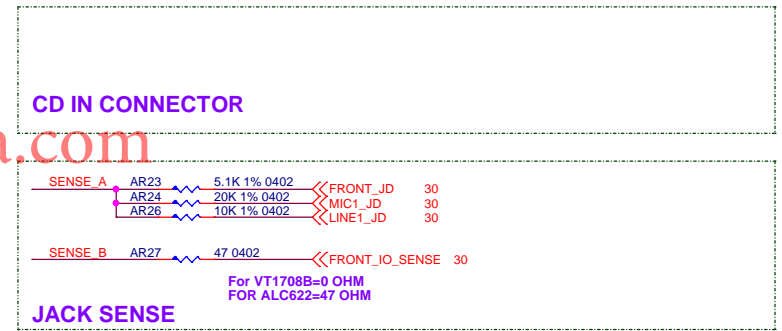
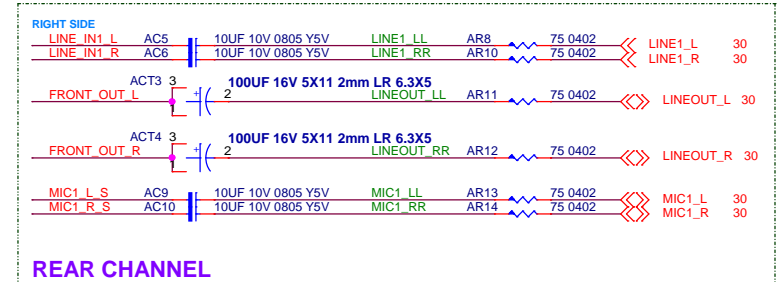
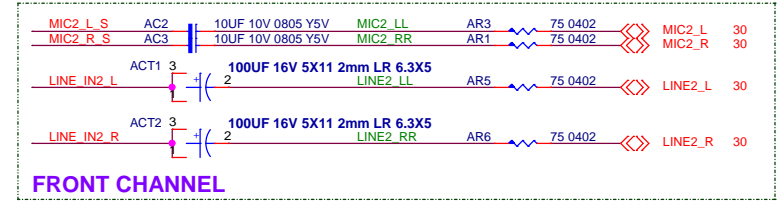
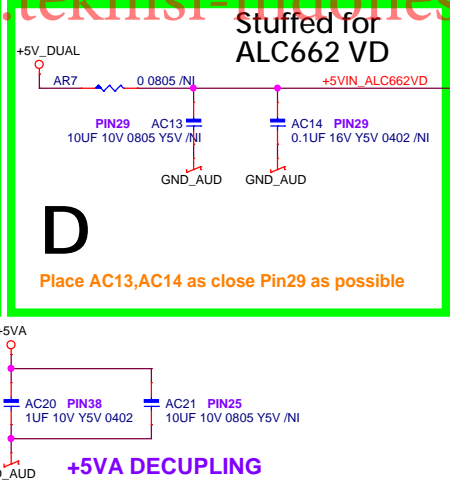
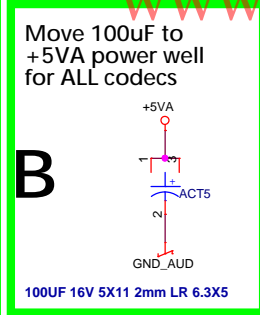
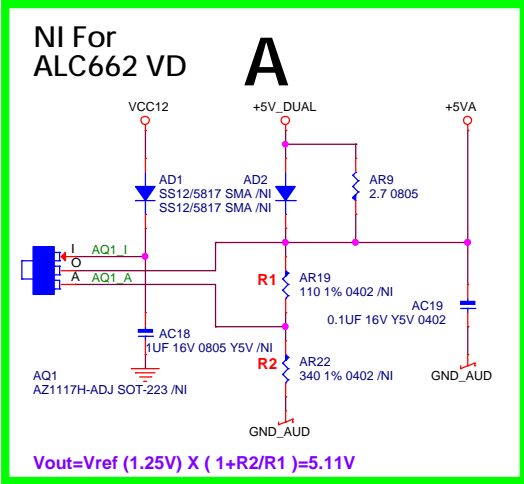
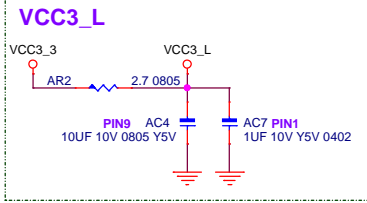
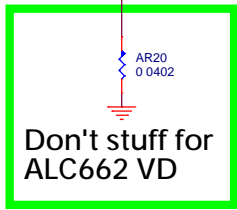
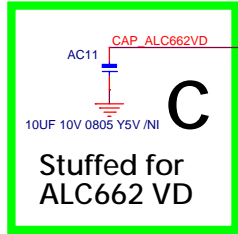
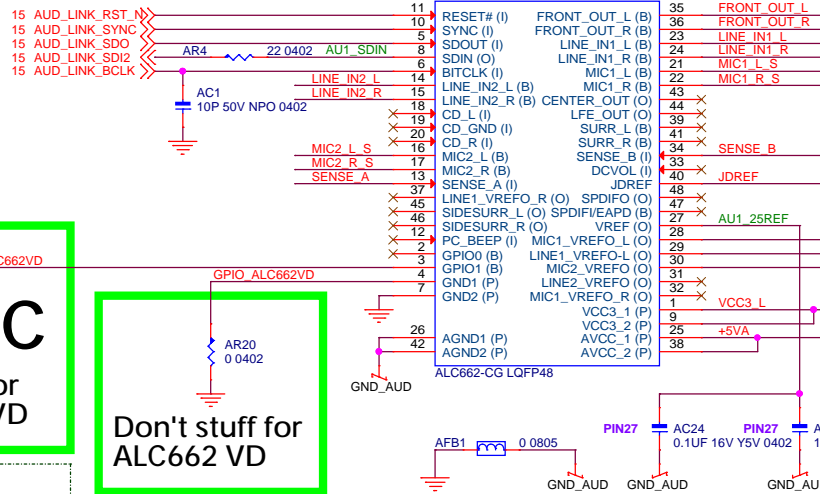
Rev: 6.0

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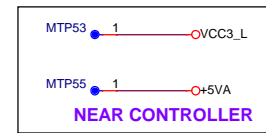
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Title RESERVED		
Size B	Document Number IH77A-MHS	Rev 6.0
Date: Monday, April 22, 2013		Sheet 28 of 47

AUDIO PART: A+Reference



FOR VT1708B LQFP48: AR30=5.1K
FOR ALC662 LQFP48: AR30=20K

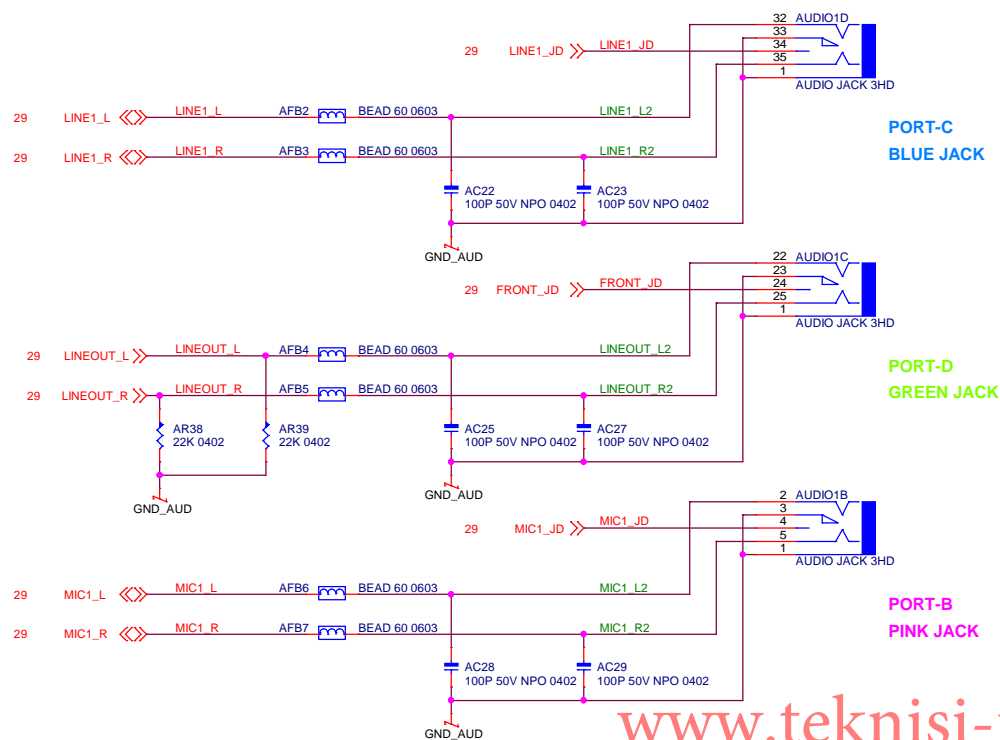


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BIOSTAR GROUP

Title **CODEC ALC662**

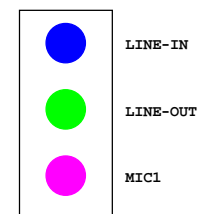
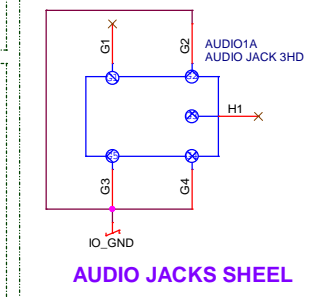
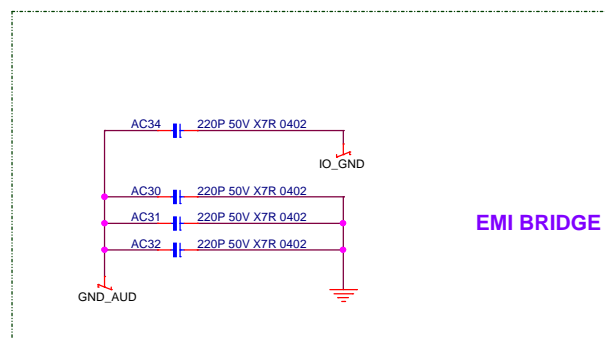
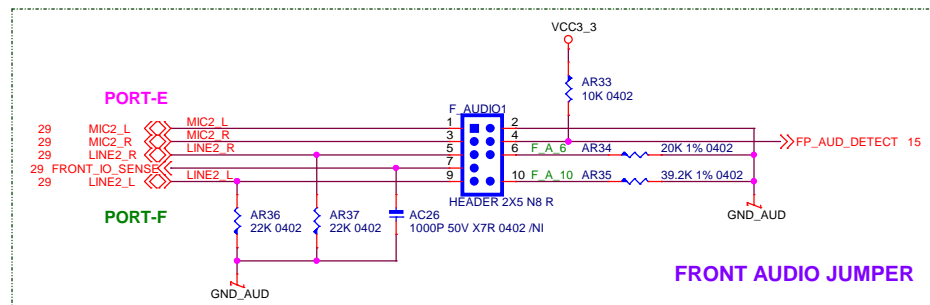
Size B Document Number **IH77A-MHS** Rev 6.0

Date: Monday, April 22, 2013 Sheet 29 of 47



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REAR AUDIO JACKS



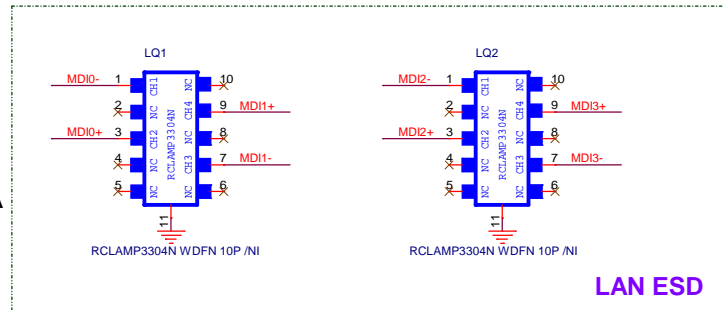
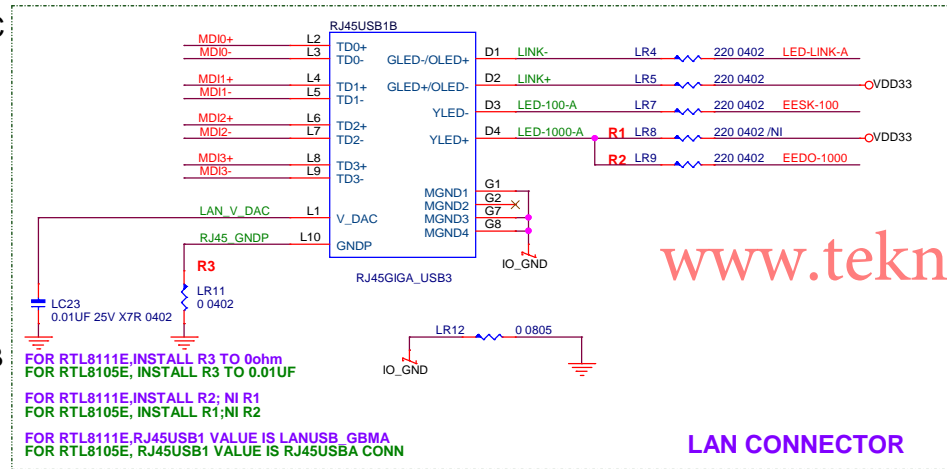
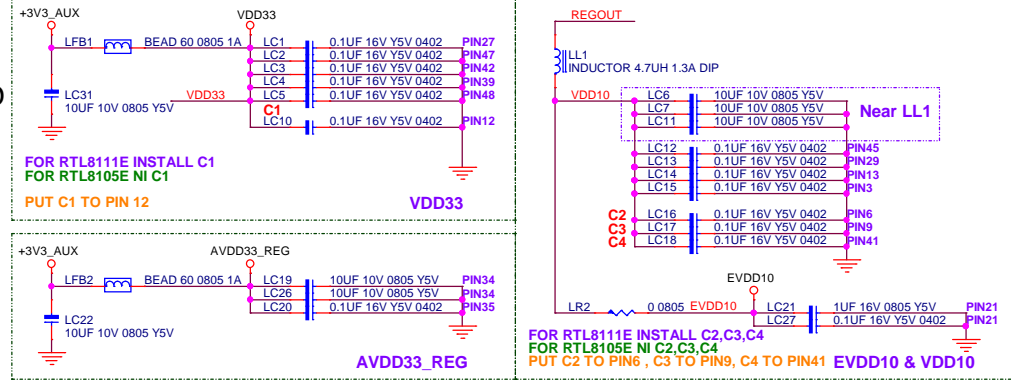
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BIOSTAR GROUP

Title: **AUDIO CONNECTOR**

Size: Custom Document Number: **IH77A-MHS** Rev: 6.0

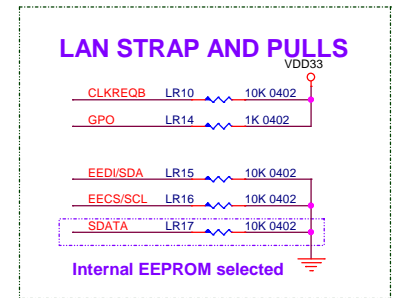
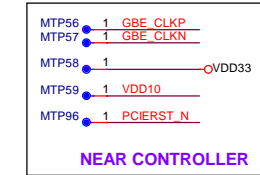
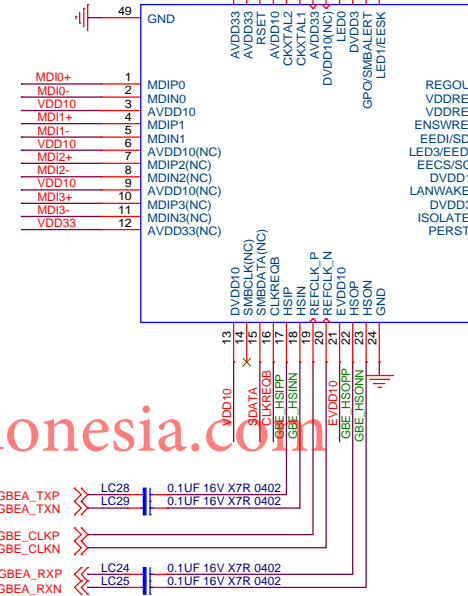
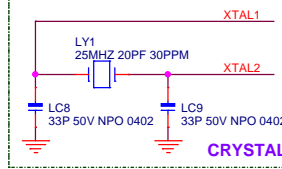
Date: Monday, April 22, 2013 Sheet: 30 of 47

LAN PART: L+Reference



COMPONENT CONTRAST LIST

LAN PARTS	C1	C2	C3	C4	R1	R2	R3	RJ45 CONN
RTL8111E	O	O	O	O	X	O	0ohm	LANUSB_GBMA
RTL8105E	X	X	X	X	O	X	0.01uF	RJ45USBA_CONN



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BIOSTAR GROUP**

File: **RTL8111E/8105E**

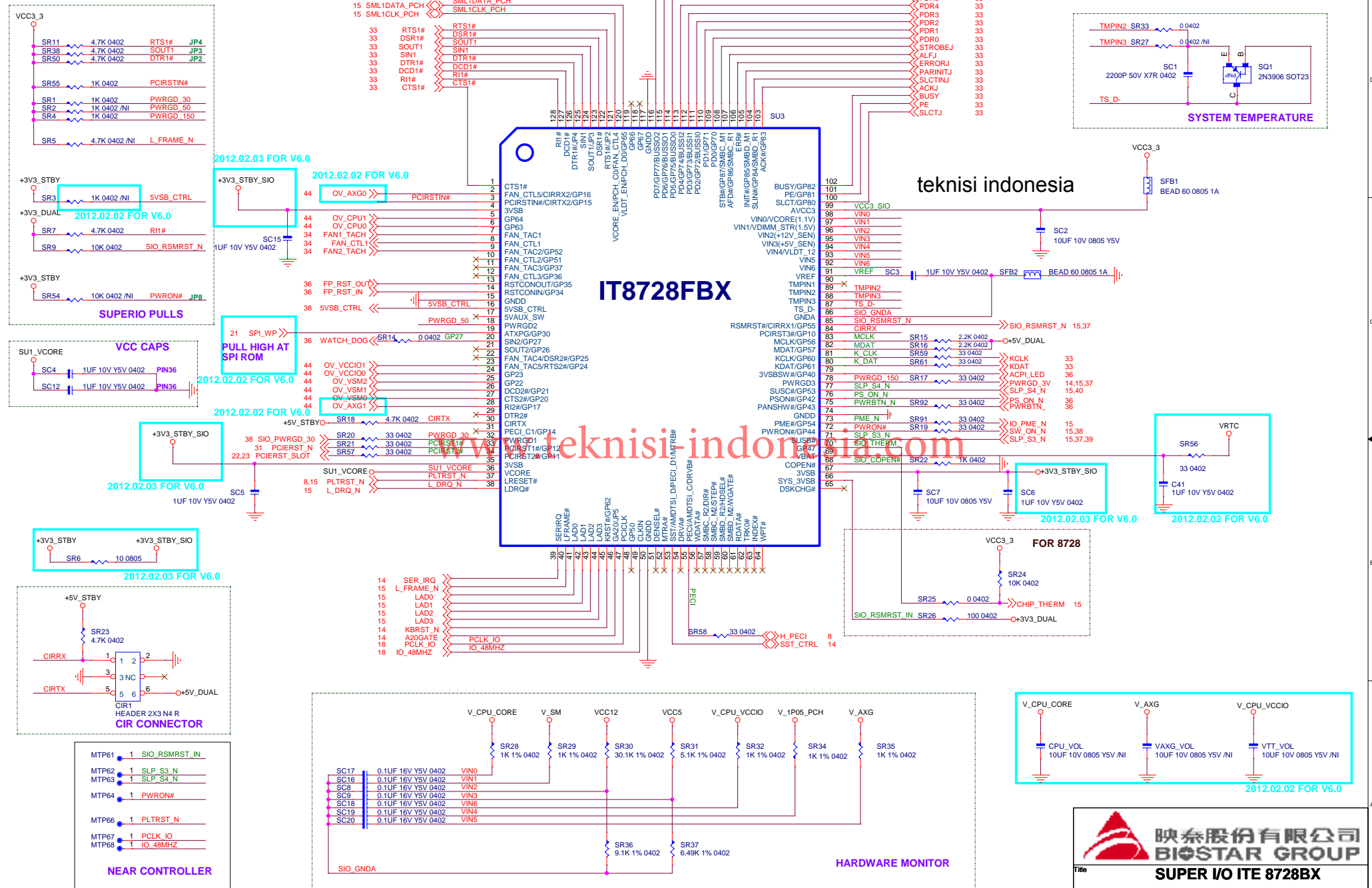
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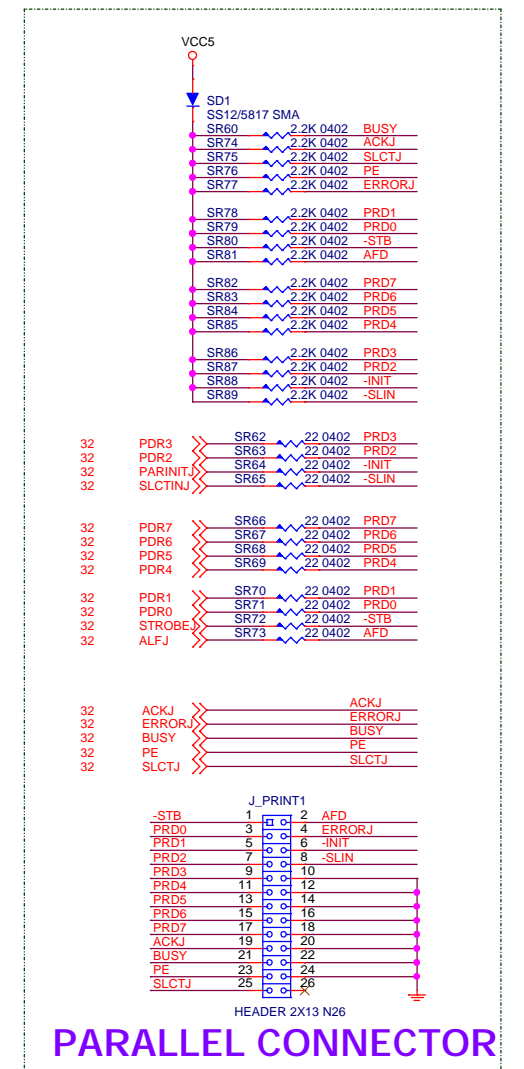
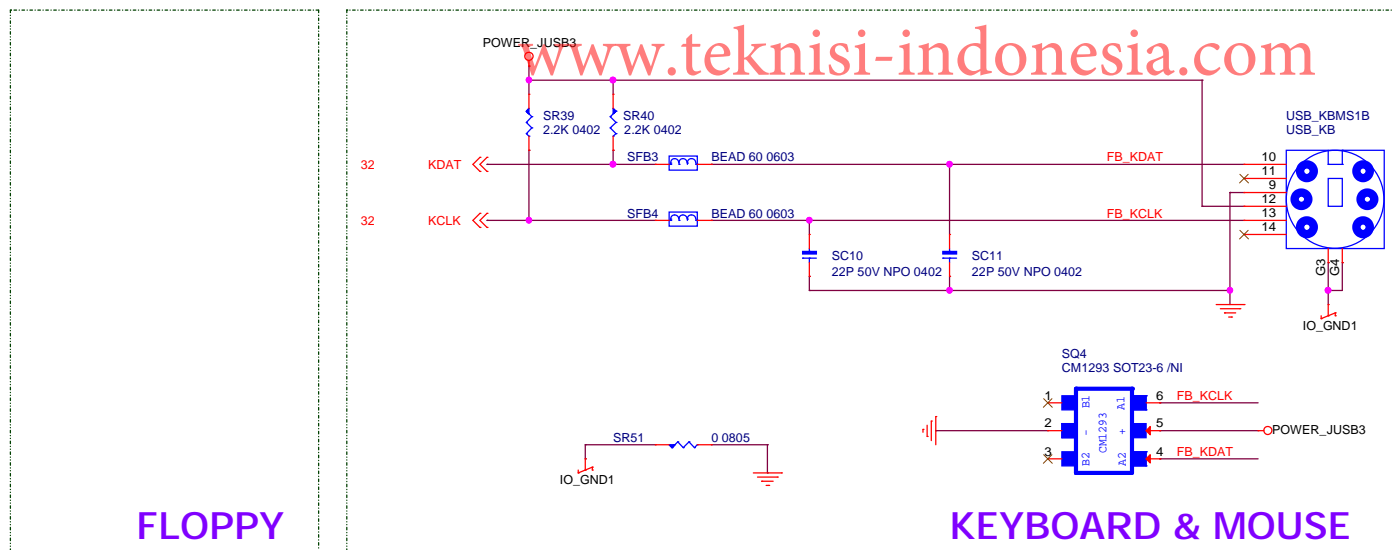
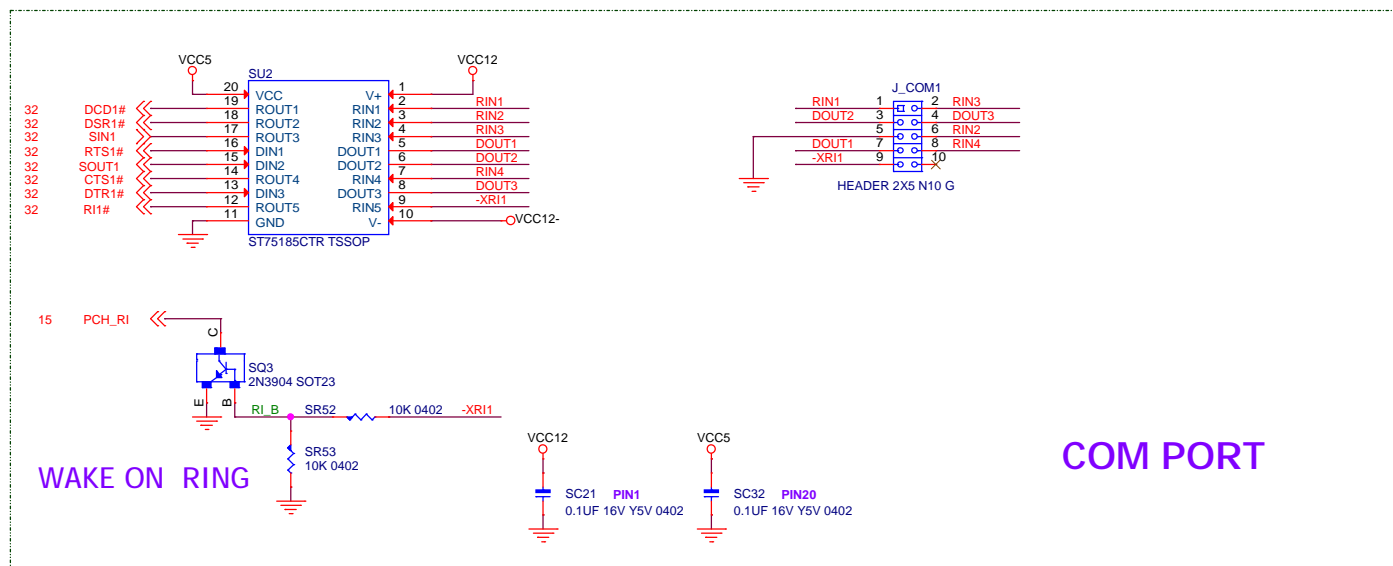
Date: **Monday, April 22, 2013**

Sheet: **31 of 47**

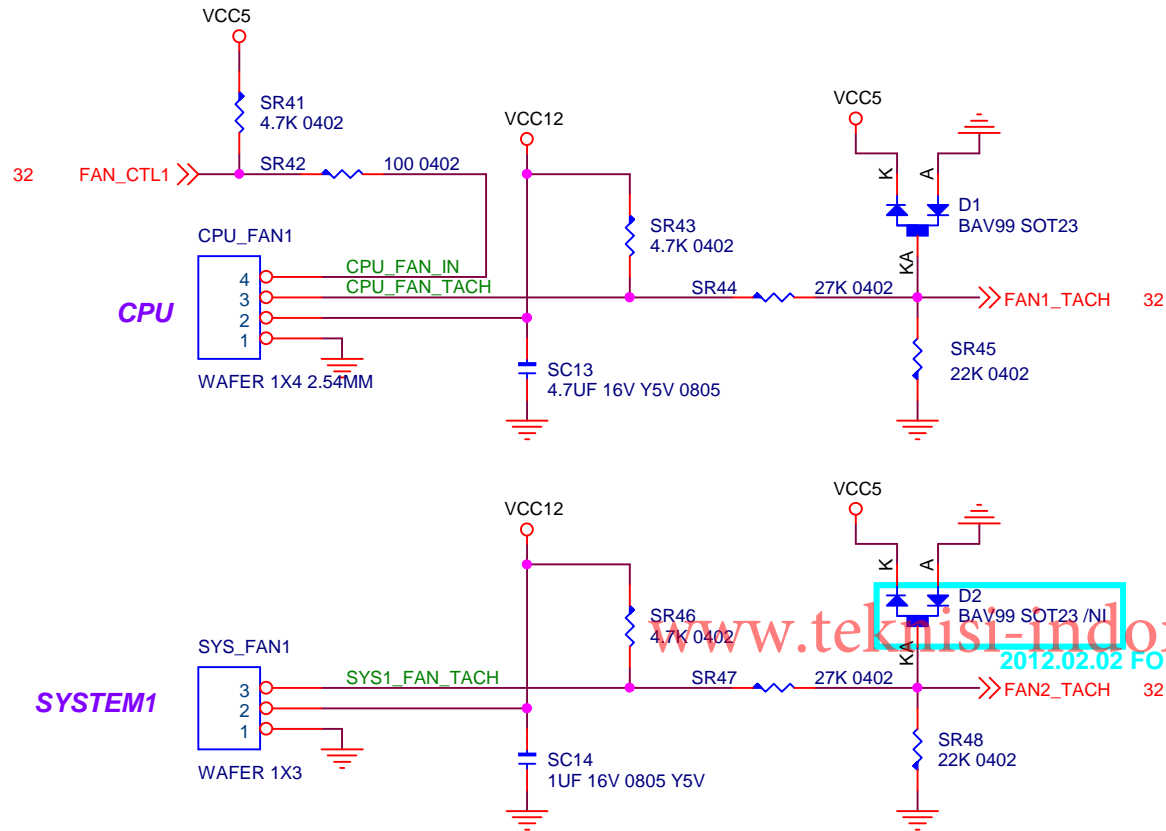
Rev: **6.0**

SUPERIO PART: S+Reference




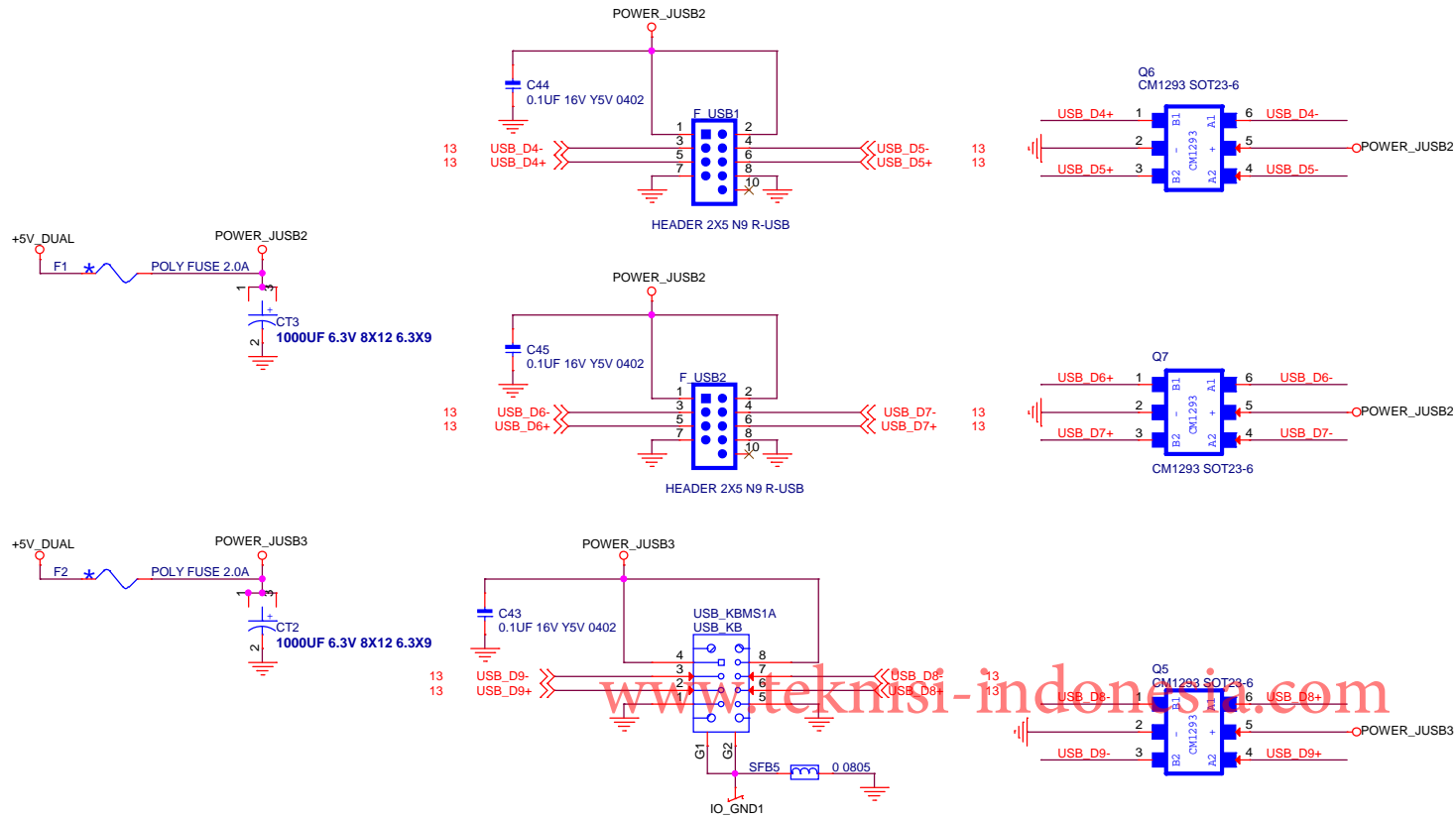


CPU FAN/SYSTEM FAN1

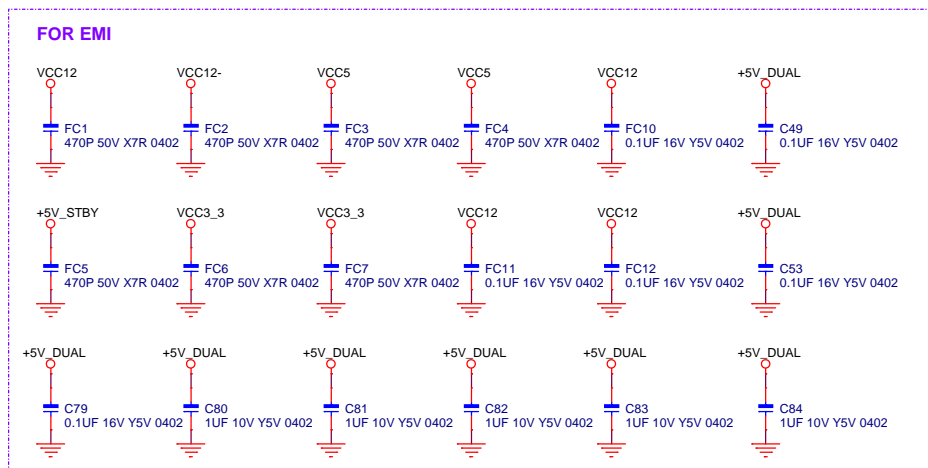
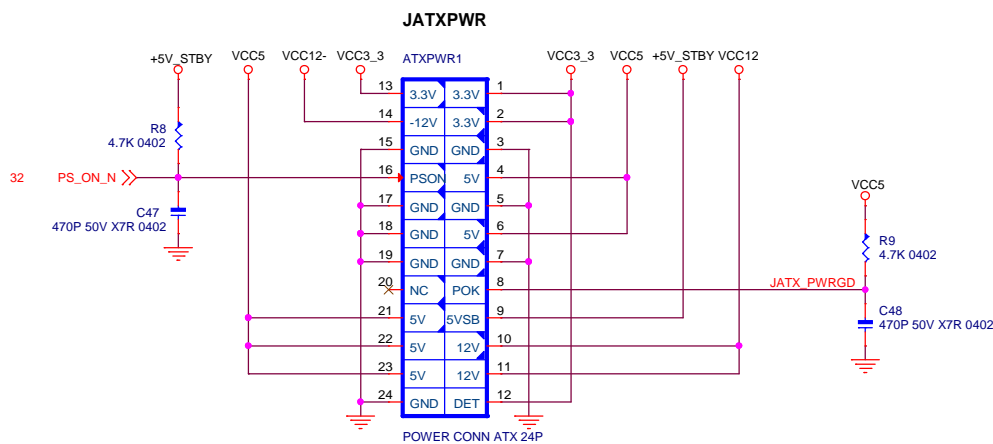


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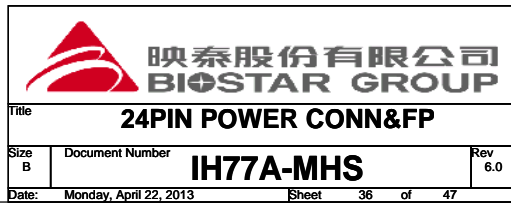
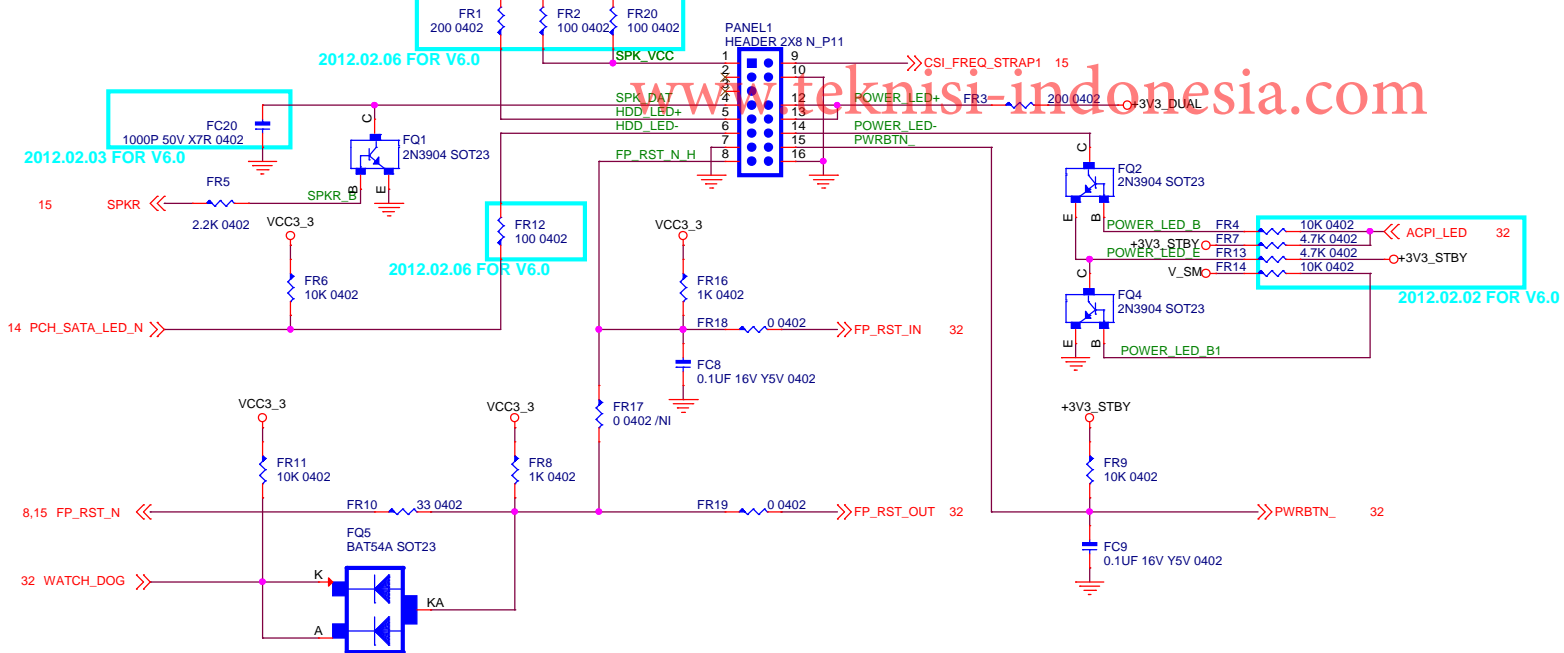
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Title FAN CONTROL		
Size A	Document Number IH77A-MHS	Rev 6.0
Date: Monday, April 22, 2013		Sheet 34 of 47

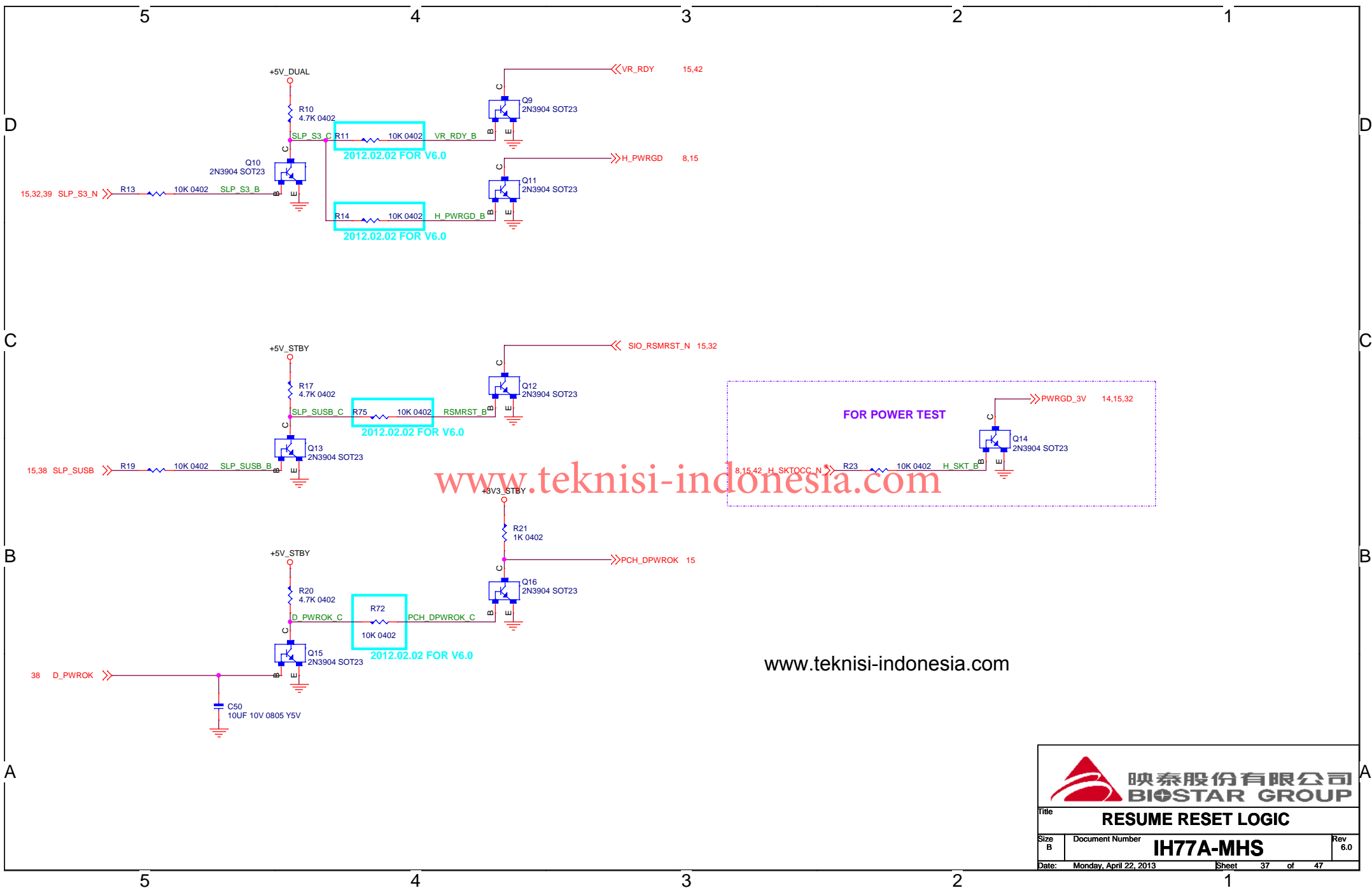


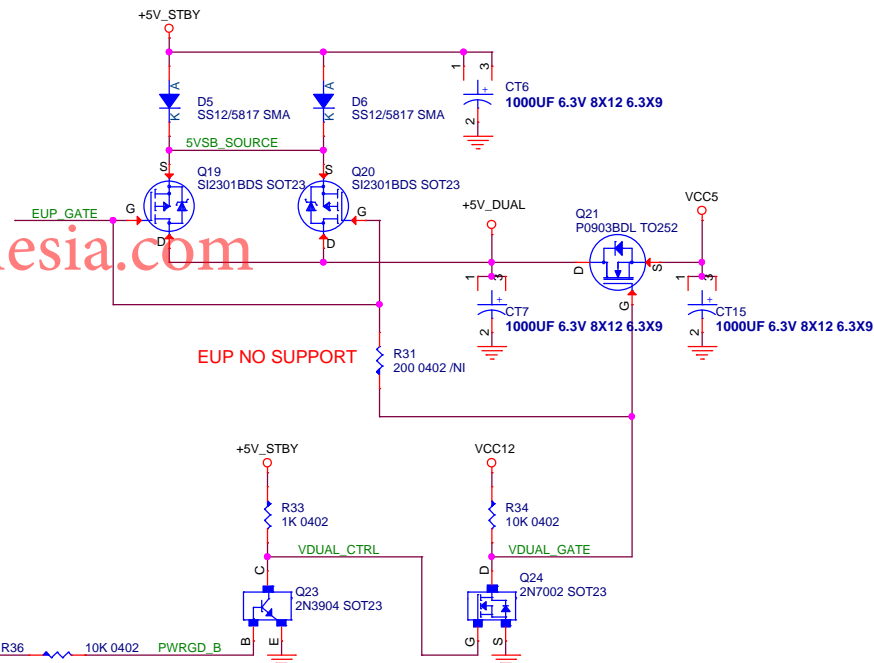
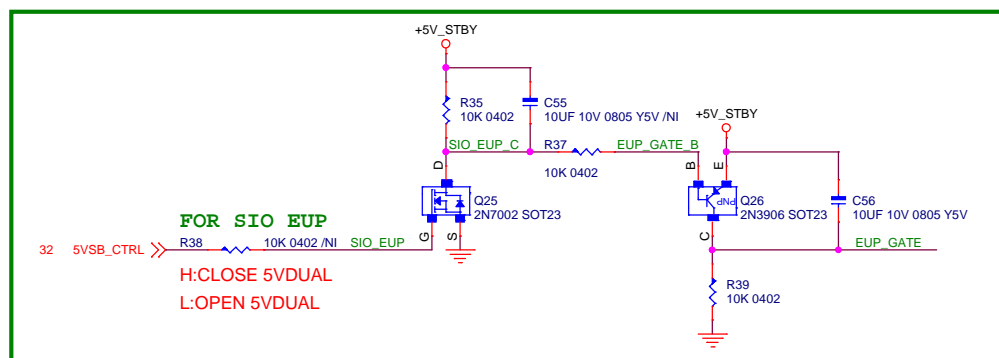
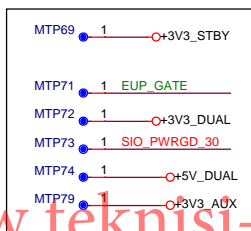
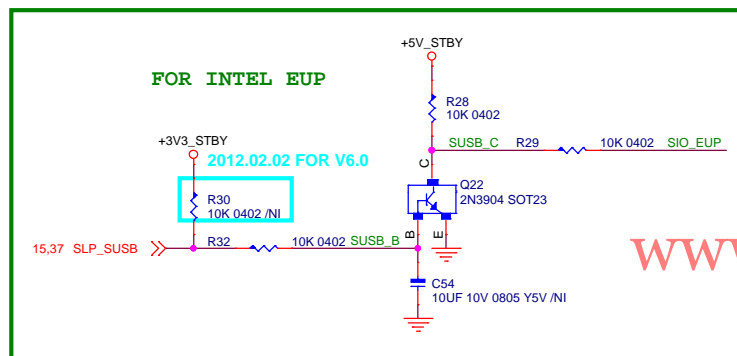
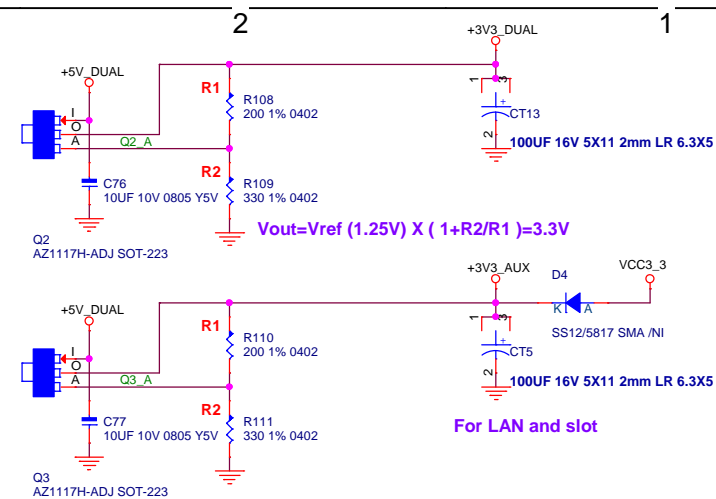
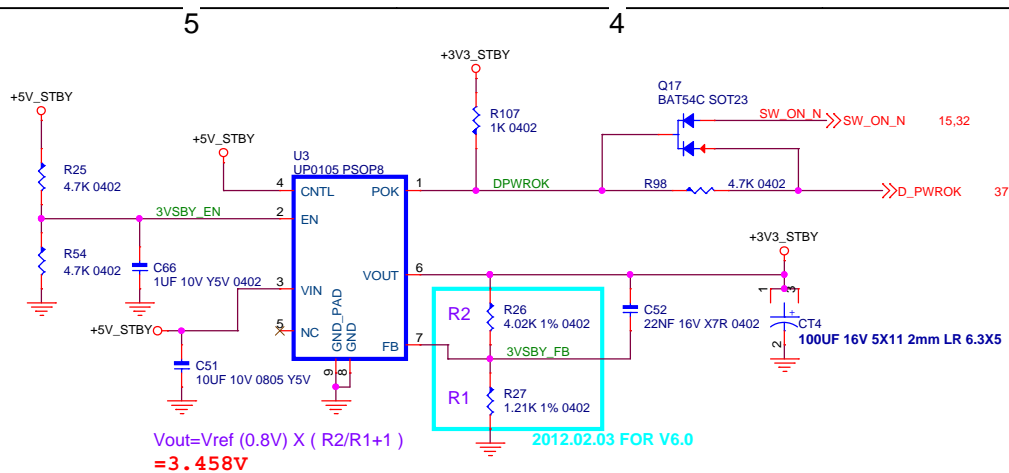
24 PIN POWER CONNECTOR



FRONT PANEL HEADER

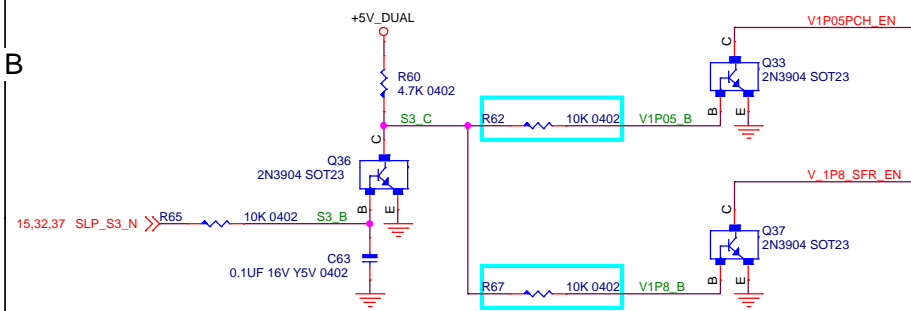
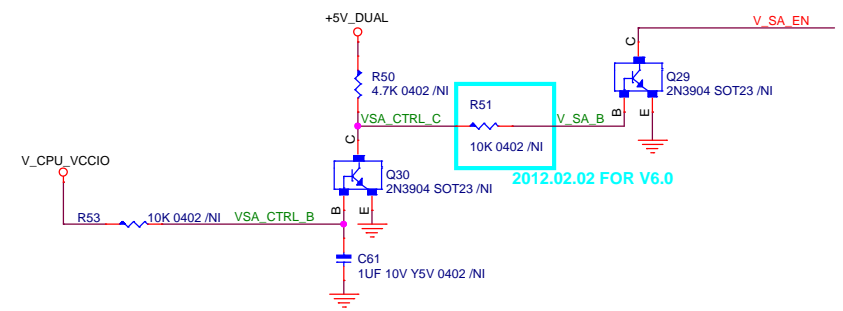
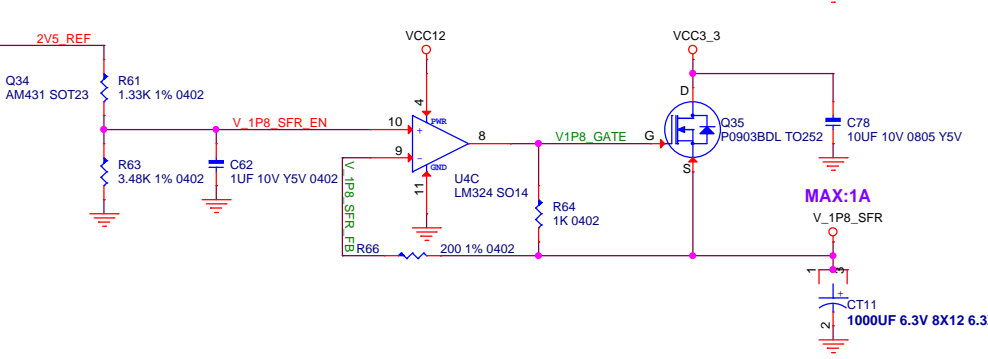
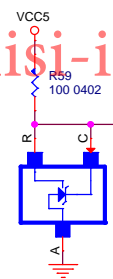
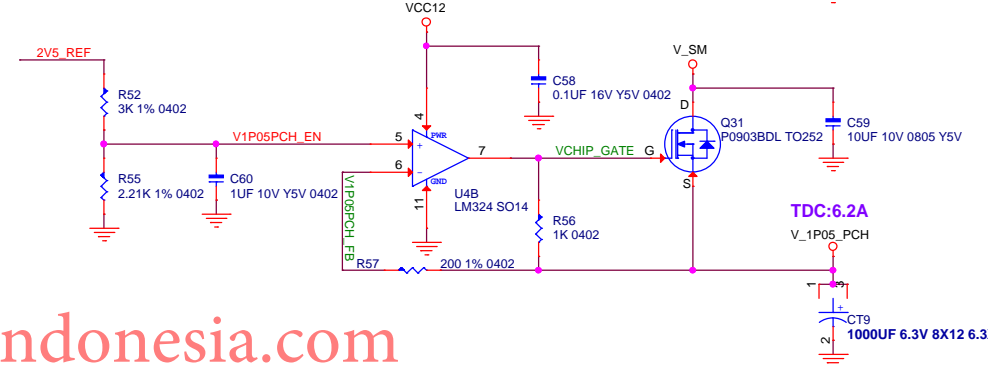
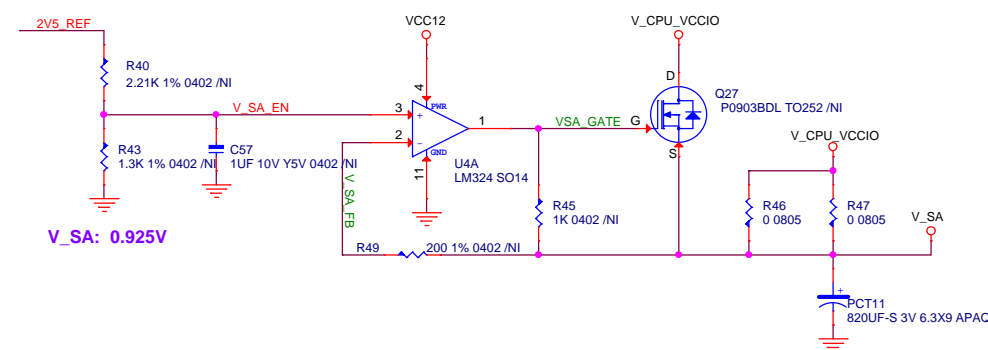






MTP76 1 V1P05PCH_EN
MTP77 1 V_1P8_SFR_EN

NEAR OP



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MEMORY VLOTAGE CONTROL CIRCUIT FOR INTEL PLATFORM

2012.02.02 FOR V6.0

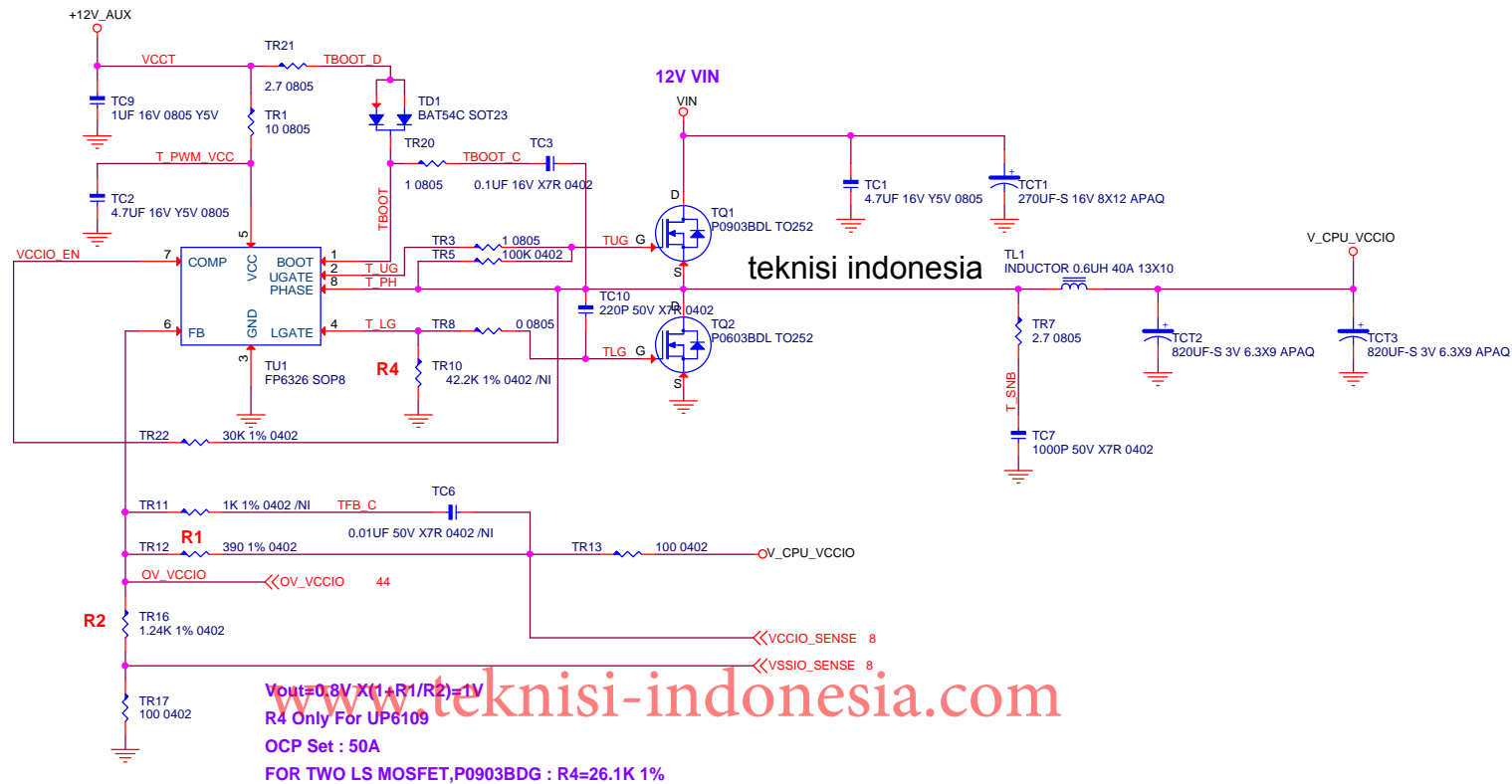
44 OV_VSM

$$V_{SM} = 0.8(1 + R1/R2) = 1.526V$$

R5 Only For FP6321A
(40uA * R5 - 0.4V) / Rds=loc
FOR ONE LS MOSFET, R5=30K 1%

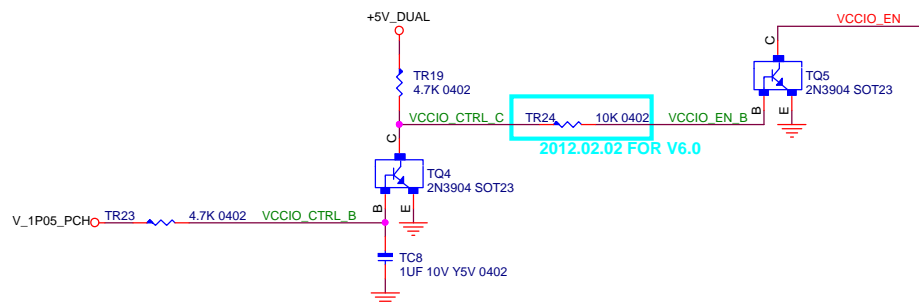
R4 Only For UP6109
OCP Set : 50A
FOR ONE LS MOSFET, P75N02LDG : R4=42.2K 1%

For T-Series----270UF-S 16V 8X11 ELITE
For NO T-Series----470UF 16V 8X11.5



MTP78 1 VCCIO_EN

NEAR CONTROLLER



PULL HIGH AT PCH
15.37 VR_RDY

8 H_VIDSOUT
8 H_VIDALERT_N
8 H_VIDSSOK_C
8 H_PROCHOT_N

44 OV_CPU

8 VCC_SENSE

8 VSS_SENSE

44 OV_AXG

8 VCCAXG_SENSE

8 VSSAXG_SENSE

Set ADDR

Set IMON

Set IMONG

Set ADDR

Set ADDR

Set ADDR

Set ADDR

Freq=200KHZ

Freq=200KHZ

Freq=200KHZ

Freq=200KHZ

Freq=200KHZ

Freq=200KHZ

Freq=200KHZ

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CONTROL PWM

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VCORE VREG1

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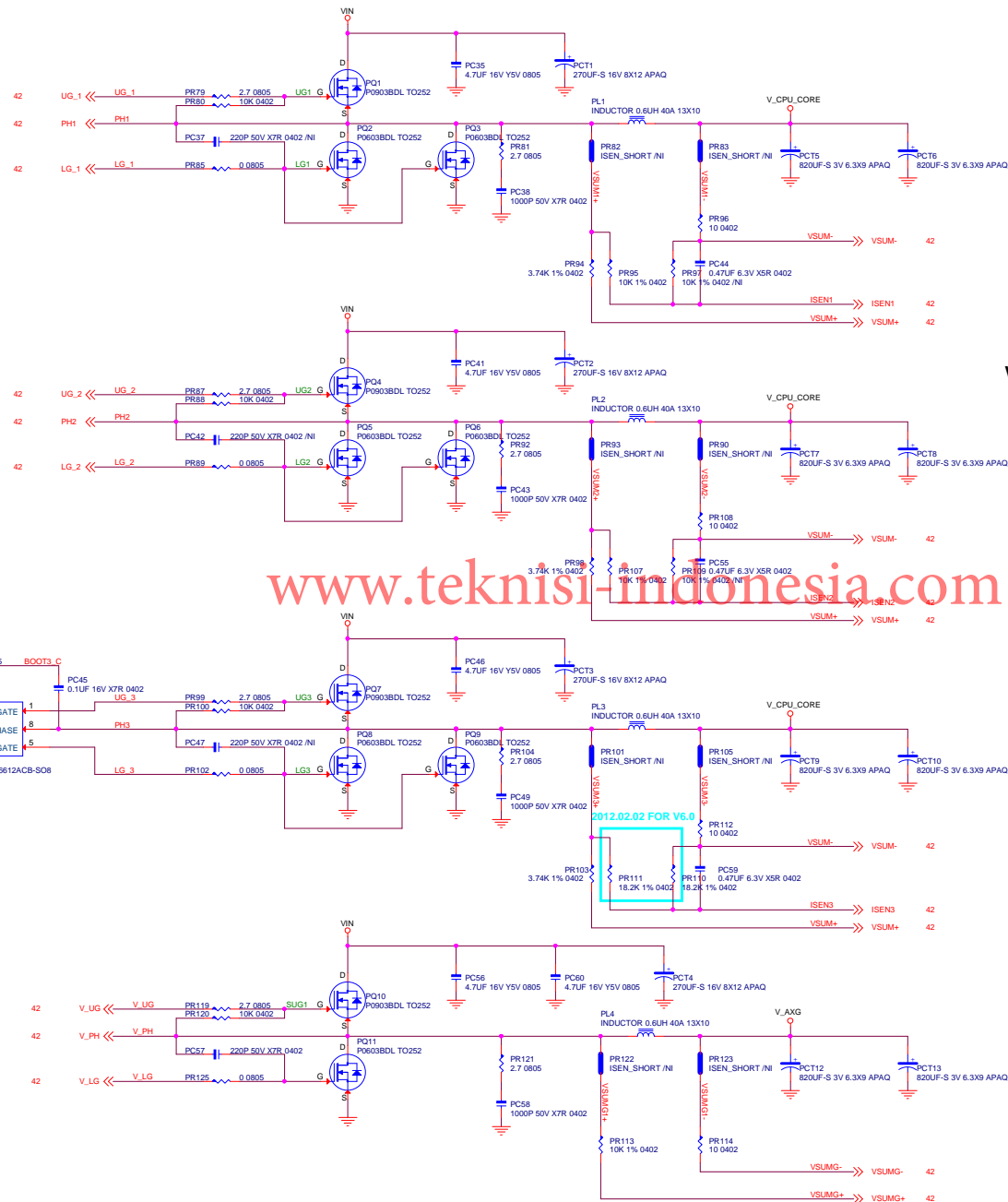
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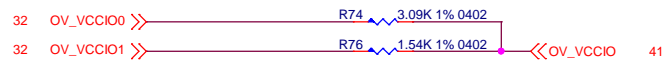
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Sheet: 42 of 47

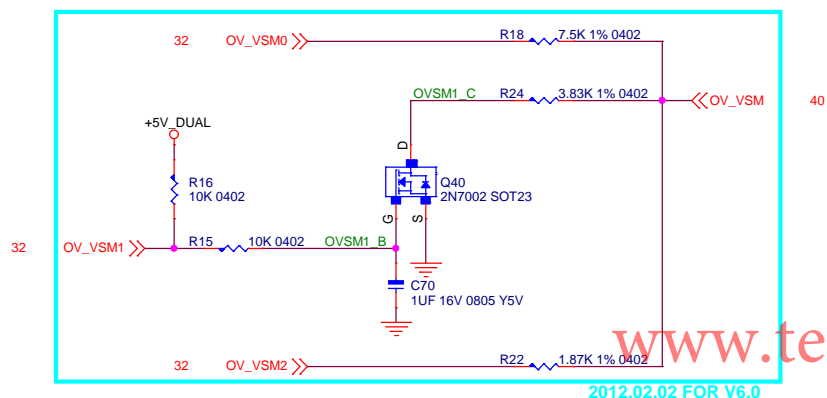


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V_CPU_VCCIO	OV_VCCIO0	OV_VCCIO1
1.05V(DEFAULT)	1	1
1.15V	0	1
1.25V	1	0
1.35V	0	0




V_SM	OV_VSM0	OV_VSM1	OV_VSM2
1.3V(1.332)	1	0	1
1.4V(1.431)	0	0	1
1.5V(DEFAULT)(1.526)	1	1	1
1.6V(1.625)	0	1	1
1.7V(1.730)	1	0	0
1.8V(1.829)	0	0	0
1.9V(1.924)	1	1	0



V_CPU_CORE	OV_CPU0	OV_CPU1
DEFAULT	1	1
+5%	0	1
+10%	1	0
+15%	0	0



V_AXG	OV_AXG0	OV_AXG1
DEFAULT	1	1
+3.3%	0	1
+6.6%	1	0
+10%	0	0



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Title: **RESERVED**

Size: Custom Document Number: **IH77A-MHS** Rev: 6.0

Date: Monday, April 22, 2013 Sheet: 44 of 47

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Custom	IH77A-MHS	6.0	
Date:	Monday, April 22, 2013	Sheet	45 of 47

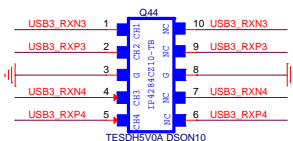
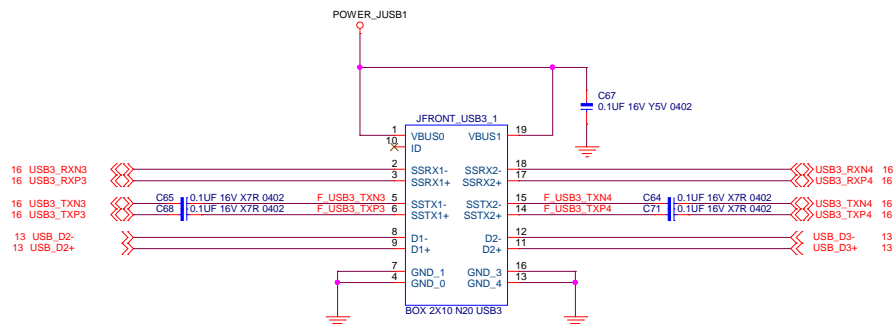
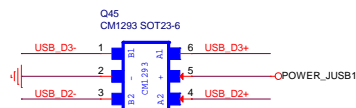
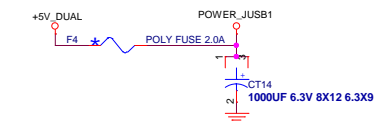
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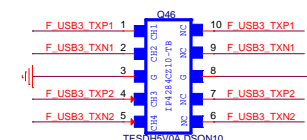
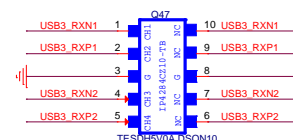
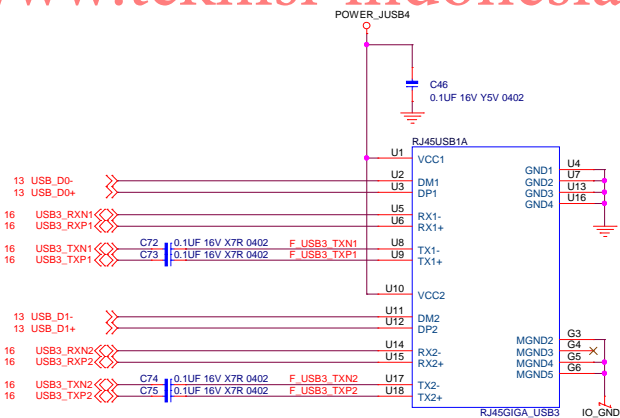
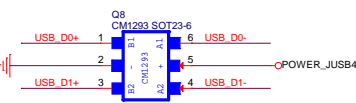
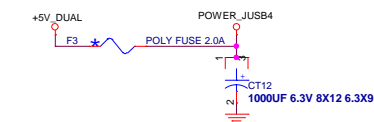
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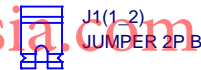
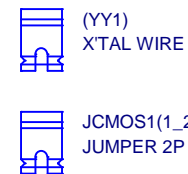
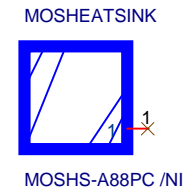
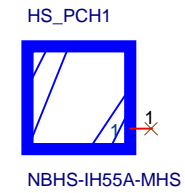
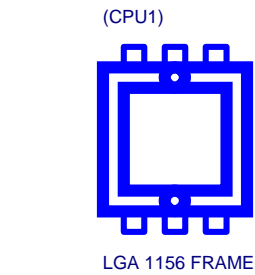
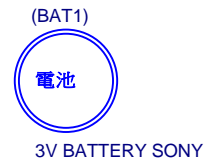
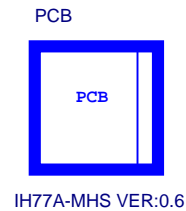
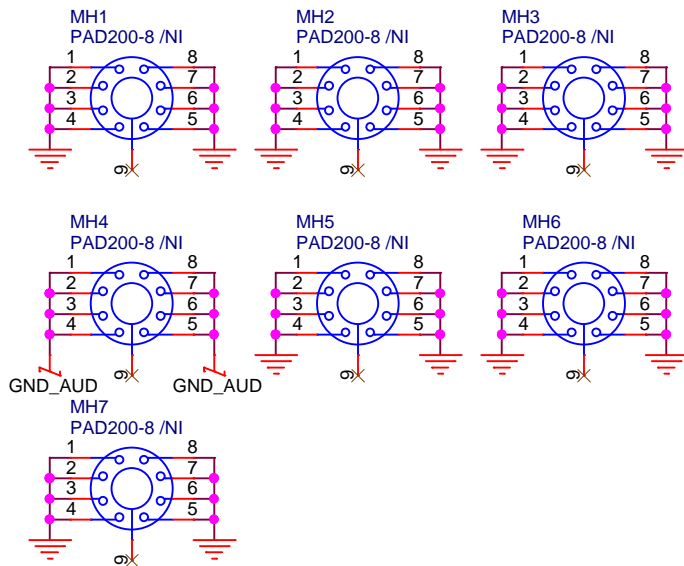
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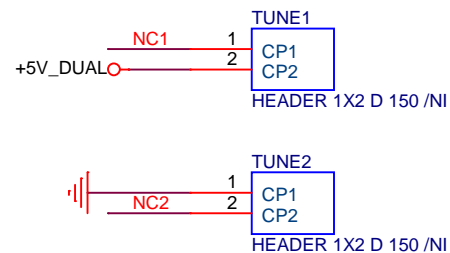




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Impedance Testing Coupon



New PANEL1
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Title			BOM
Size	Document Number	IH77A-MHS	
A		Rev 6.0	
Date:	Monday, April 22, 2013	Sheet	47 of 47